



basic education

Department:
Basic Education
REPUBLIC OF SOUTH AFRICA

ELECTRICAL TECHNOLOGY (ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS

GRADE 12

2021

These guidelines consist of 44 pages.

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1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- **AGRICULTURE:** Agricultural Management Practices, Agricultural Technology
- **ARTS:** Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- **SCIENCES:** Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- **SERVICES:** Consumer Studies, Hospitality Studies, Tourism
- **TECHNOLOGY:** Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps need to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for electronics.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2021 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
 - Enclosure:
 - The file must include a design.
 - The enclosure and the design must match.
 - No cardboard boxes are allowed.
 - Plastic, wooden and metal enclosures are acceptable.
 - Enclosures that are manufactured and/or assembled by the learners are preferred.
 - The enclosure should be accessible for scrutiny inside.
 - Lids that are secured are preferred.

- Circuit board:
 - The file should include the PCB design.
 - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
 - Switches, potentiometers, connectors and other items must be mounted.
 - Wiring must be neat and bound/wrapped.
 - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
- Logo and name:
 - The file should contain the logo and name design and specification plate.
 - Logo, specification plate and name must be prominent on the enclosure.
 - The logo/specification plate must be affixed in a permanent manner – painted, glued or stuck on with vinyl

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the **FIRST THREE TERMS** and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must not be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a **working model and model answer file** that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. **No re-assessment will be done once the facet sheets have been completed** and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2021	Teacher – Builds the models and works out the model answers for the simulations for 2021. Identifies shortages in tools, equipment and consumable items for simulations that must be procured in 2021. SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2021	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
January 2021	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to
February 2021	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2021	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
April–June 2021	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate simulation 1 10% of learners' work is moderated
April–June 2021	PAT project – learners continue with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2021	PAT intervention	Learners that are behind on the PAT are required to complete the project during this holiday.
July–August 2021	Moderation of Simulation 2	District subject facilitator/subject specialist will visit the school and moderate simulation 2 – different learners from the previous term 10% of learners' work is moderated
July–August 2021	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed
September–October 2021	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly

2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulation 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. Both simulations will be moderated.
- **The teacher is required to build an exemplar model for each project type chosen for the school.**
- **This model must be on display during moderation.**
- **The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).**
- **Level 5 assessments must exceed the model of the teacher in skill and finishing.**
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- **If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.**
- The moderator will randomly select no fewer than **two projects** (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of Tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who make use of simulation programs on a computer may use it for the learners to practice on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

- STEP 1: The teacher will choose simulations from the provided examples.
- STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items are lost/damaged very easily when learners work with them.
- STEP 3: Contact three different electronics component suppliers for comparative quotations.
- STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
- STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
- STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/resource availability.

Teachers are required to develop a set of model answers in the teacher's file.

Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided from schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects are varied in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They **MUST** redraw these circuits in their file correctly.

The description of the operation of the circuits is NOT complete. It is required of learners to interrogate the function of the components in the provided circuit. They should elaborate on the purpose of components in the circuit. It is recommended that those learners investigate similar circuits available on the internet and in the school library or workshop reference books.

2.8 Working mark sheet

(A working Excel file is provided with this PAT)

PAT mark sheet		Term 1	Term 2	Project		Total = Term 1 + Term 2 + Project 250	Mark out of 100	Moderated Mark
No.	Name of Learner	Simulation 1 50	Simulation 2 50	Design and Make Part 1 120	Design and Make Part 2 30			
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
	Total							
	Average							

Teacher Name: _____

Principal Name: _____

Moderator Name: _____

Signature: _____

Signature: _____

Signature: _____

Date: _____

Date: _____

Date: _____

3. LEARNER GUIDELINES

PAT 2021 cover page (Place this page at the front of the PAT.)

**Department of Basic Education
Grade 12
CAPS for Technical High Schools
Practical Assessment Task – Electrical Technology**

Time allowed: Terms 1–3 (2021)

Learner Name: _____

Class: _____

School: _____

Specialisation: ELECTRONICS**Complete TWO simulations.****Project (Write the name of the project):** _____**Evidence of moderation:****NOTE:**

When the learner evidence (LE) selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation 1	50		
Simulation 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
Total	250		

3.1 Instructions to learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work and co-operative work is not allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain **2** simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO digits. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and can be in colour or greyscale. Scanned photos and photocopies are allowed.
- This document must be placed inside your PAT file together with the other evidence.
- Learners with identical photos will be penalised and receive zero for that section

3.2 Declaration of Authenticity (COMPULSORY)

Declaration:

I _____ herewith declare that the work represented in this evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

Signature of learner

Date

4. SIMULATIONS**4.1 Simulation 1: RLC series circuit**

Name of learner: _____		Mark <div style="border: 1px solid black; width: 60px; height: 60px; margin: 0 auto; display: flex; align-items: center; justify-content: center;"> — 50 — </div>
Class: _____	Date Completed: _____	
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

4.1.1 Purpose:

- To understand the operation of a resistor, inductor and capacitor in a series circuit with an AC supply.
- To understand resonant frequency.
- To compare the measured and the calculated values.

4.1.2 Procedure:

Build the series RLC circuit in FIGURE 4.1.4 on the breadboard using the components provided.

Connect the circuit to a function generator.

Set the output signal voltage of the function generator to 3 V peak to peak with a frequency of 1 kHz.

4.1.3 Required resources:

COMPONENTS	TOOLS AND EQUIPMENT
$R_1 = 1 \text{ k}\Omega$ resistor $L_1 = 1 \text{ }\mu\text{H}$ inductor $C_1 = 1 \text{ }\mu\text{F}$ capacitor	Multimeter Function generator Leads Breadboard Side cutters Pair of pliers Oscilloscope

4.1.4 **Circuit diagram:**

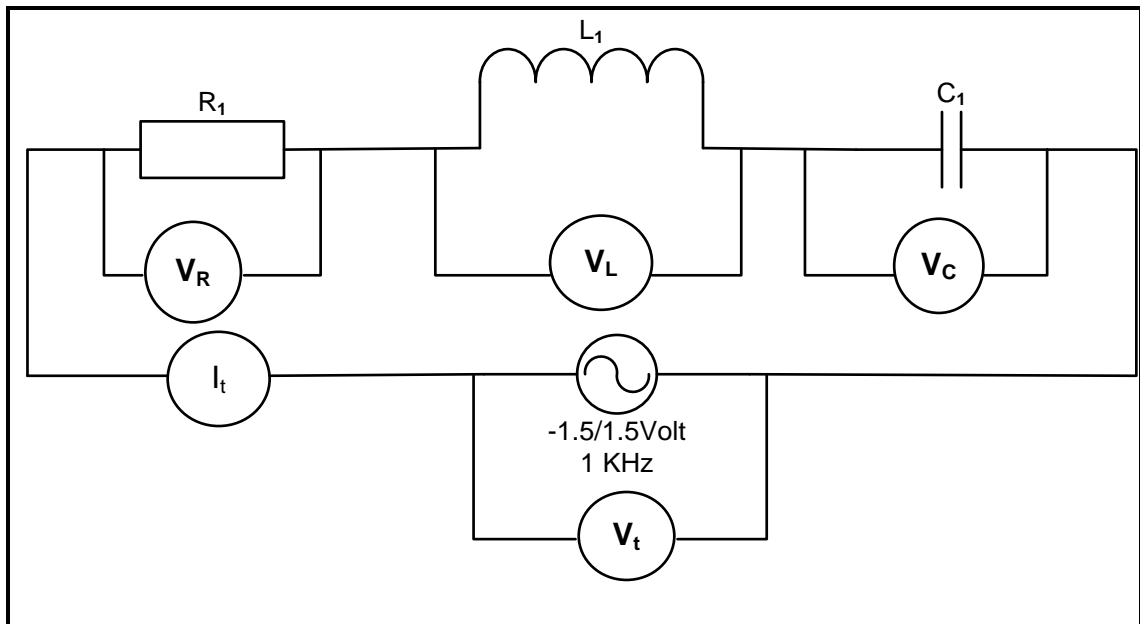


FIGURE 4.1.4: RLC CIRCUIT DIAGRAM

4.1.5 Complete TABLE 4.1.5 by entering values of V_R , V_L , V_C , V_T , and I_T measured.
NOTE: Alternatively measure with the oscilloscope and convert to V_{rms} values.

METERS CONNECTED ACROSS	MEASUREMENTS
V_R	
V_L	
V_C	
V_T	
I_T	

TABLE 4.1.5

(5)

4.1.6 Calculate the following:

(a) The inductive reactance of the inductor.

(3)

(b) The capacitive reactance of the capacitor (3)

(c) The impedance of the circuit (3)

(d) The total current in the circuit using calculated values. (3)

(e) The voltage drop across the resistor using calculated values. (3)

(f) The voltage drop across the inductor using calculated values. (3)

(g) The voltage drop across the capacitor using calculated values. (3)

(h) The resonant frequency for the circuit. (3)

4.1.7 Compare the measured values with the calculated values and enter the values in the table below:

QUANTITIES		MEASURED VALUES	CALCULATED VALUES
(a)	Total current		
(b)	Resistor voltage		
(c)	Inductor voltage		
(d)	Capacitor voltage		
(e)	V_{XC} at resonance		
(f)	V_{XL} at resonance		

Are the measured and calculated values the same? Yes or No.
Motive:

(2)

4.1.8 Set the function generator to the resonant frequency and record the value of:

(4)

$V_{XC} =$ _____ (V)

$V_{XL} =$ _____ (V)

$V_R =$ _____ (V)

$I_T =$ _____ (A)

4.1.9 Write a conclusion about the measurements observed in QUESTION 4.1.8 when the circuit is at resonance.

(3)

Subtotal: (38)

LEVEL DESCRIPTOR				MARKS OBTAINED
0	1	2	4	
The candidate was not able to build the circuit on his own.	The candidate was able to partially build the circuit on his own.	The candidate was able to correctly build the circuit with the assistance of the teacher.	The candidate built the circuit correctly without the assistance of the teacher.	
The candidate was not able to connect the measuring instruments.	The candidate was able to partially connect the measuring instruments to the circuit.	The candidate connected the measuring instruments correctly and measured the voltages and currents with the assistance of the teacher.	The candidate connected the measuring instruments correctly and measured the voltages and currents on his own.	

(12)

Total: [50]

4.2 Simulation 2A: JFET amplifier circuit

Name of learner: _____		Mark <div style="border: 1px solid black; width: 60px; height: 60px; margin: 0 auto; display: flex; align-items: center; justify-content: center;"> 50 </div>
Class: _____	Date Completed: _____	
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

4.2.1 Purpose:

Build the JFET amplifier circuit in FIGURE 4.2.3 on a breadboard and investigate the advantage of using a Darlington pair compared to a single transistor. Display the input/output waveforms on an oscilloscope.

4.2.1 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	2 x 1 k Ω resistors
Analogue/Digital oscilloscope	1 x 100 Ω resistor
Function generator	1 x 100 k Ω resistor
Variable DC power supply	1 x 2k2 Ω resistor
Side cutters	1 x 750 Ω resistor
Wire stripper	1 x 10 k Ω resistor
Multimeter	1 x 22 nF capacitor (223)
	1 x 10 μ F electrolytic capacitor 32 V
	1 x 2N5457 JFET (2N5459 or 2N3819)
	Connecting wires

4.2.3 Procedure:

- (a) Build the circuit in FIGURE 4.2.3 on an experiment board.

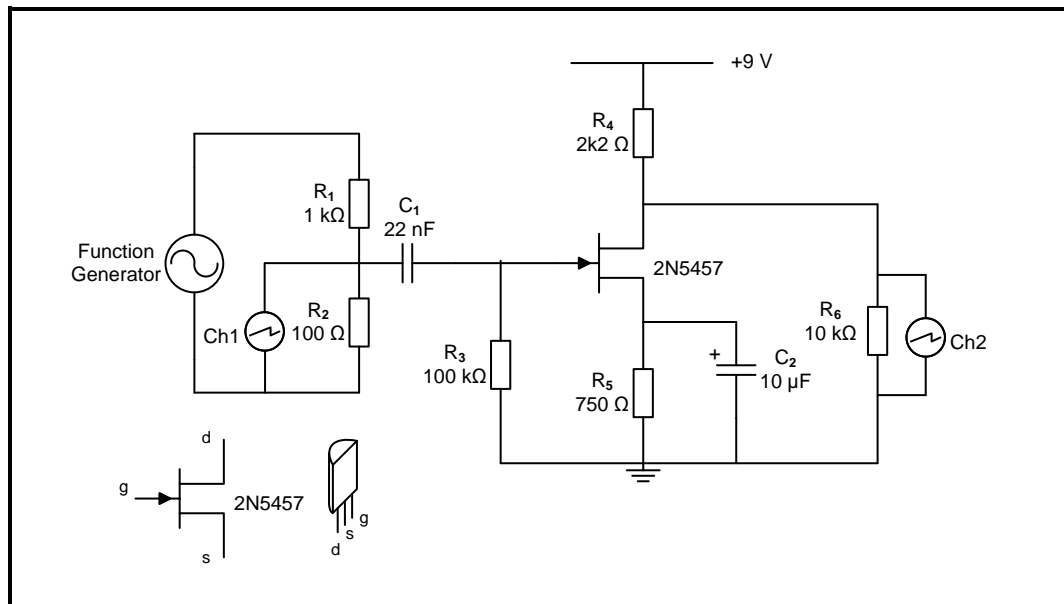
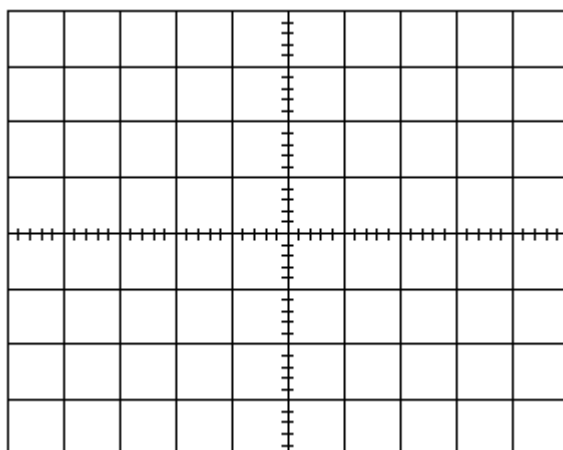


FIGURE 4.2.3: JFET AMPLIFIER CIRCUIT

- (b) Connect the function generator across R_1 and R_2 and adjust it to provide a 1 V peak to peak sine wave. (If the output saturates, decrease the input voltage to obtain an undistorted output.)
- (c) Connect channel 1 of the oscilloscope across R_2 and draw the waveform on the grid provided to scale.
- (d) Connect channel 2 of the oscilloscope across the output of the amplifier and draw the waveform on the grid provided to scale.



V/Div: _____ (Ch 1)

V/Div: _____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform and 1 mark for each correct oscilloscope setting.

(5)

- (e) Make use of the oscilloscope settings and determine the peak value of the input and output signals. (3)

$V_{IN(peak)} =$ _____

$V_{OUT(peak)} =$ _____

Phase shift between input and output? (Y/N): _____

- (f) Calculate the gain of the amplifier.

(3)

- (g) Compare the two waveforms and write a conclusion regarding the circuit.

(4)

Simulation 2A: (15)

FACET SHEET OF SIMULATION 2A: JFET AMPLIFIER CIRCUIT

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments–oscilloscope (1)	Collect hand tools (1)	4/4 = 1	
Hand tools	Use side cutters correctly (1)	Use wire stripper correctly (1)	Use long-nose pliers correctly (1)		3/3 = 1	
Preparation for insertion of components into breadboard.	Check the datasheet on the FET (1)	Set supply voltage correct at +9 V (1)	Set input voltage correct at 1 V from function generator (1)		3	
Correct connection on breadboard – nodes and polarity	Connect 6 nodes correctly (6/2 = 3)	Polarity of JFET correct (2)	Polarity of C ₂ – correct (1)		6/2 = 3	
Connection of instruments	Correct setting of the function generator (2)	Correct setting of the oscilloscope (2)	Correct connection of the oscilloscope (2)		6/2 = 3	
Circuit is working correct	Output amplified (1)	Output phase vs. input phase (1)			2	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in their places after work (1)			2/2 = 1	
Safety	Observing safety before being reminded (2)				2/2 = 1	
FACET sheet of Simulation 2A:					15	

Simulation 2B: Darlington pair current amplifier

4.2.4 Resources

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	2 x BC 109 NPN transistors
Analogue/Digital function generator	1 x LED
Variable DC power supply	1 x 560 Ω resistor
Side cutters	1 x 100 kΩ resistor
Wire stripper	Connecting wires

4.2.5 Procedure:

- (a) Construct the circuit in FIGURE 4.2.5 on an experiment board.

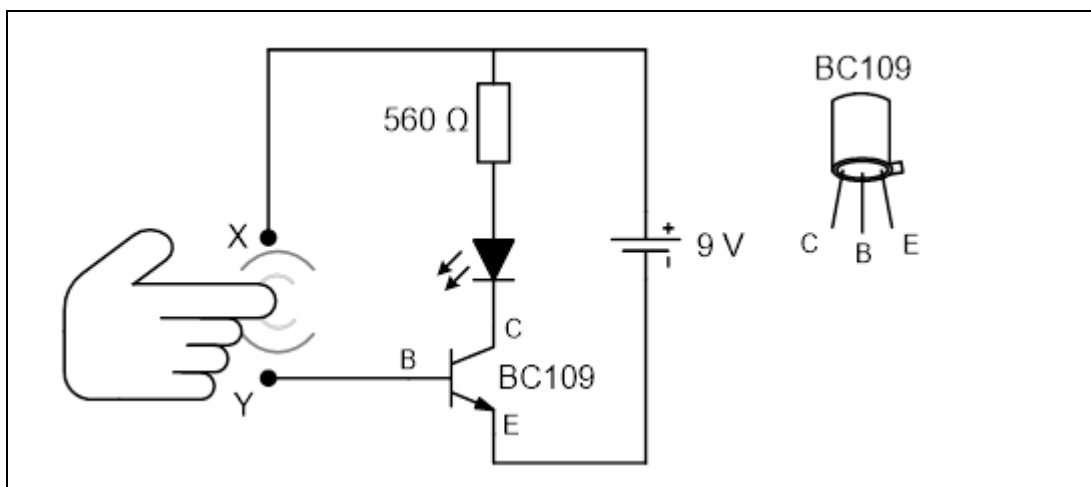


FIGURE 4.2.5: TRANSISTOR CIRCUIT

- (b) Use your finger as a pathway for the current to connect points X and Y. Once your finger is connected, observe the brightness of the LED and record your findings. Connect an ammeter between the resistor and LED.

(2)

- (c) Replace the single transistor with two identical BC109 transistors, as indicated in FIGURE 4.2.6.

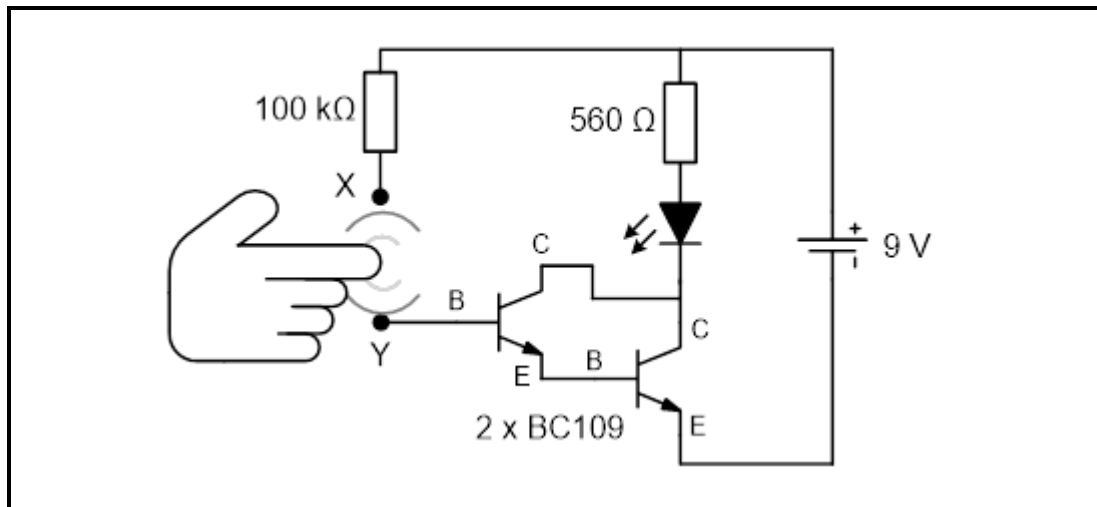


FIGURE 4.2.6: DARLINGTON PAIR

- (d) Connect points X and Y with your finger. Write down your observation of the brightness of the LED. Connect an ammeter between the resistor and LED.

(2)

- (e) Compare the brightness of the LED when one transistor is used and when two transistors are used. Motivate why this happens.

(2)

(6)

FACET SHEET OF SIMULATION 2B: DARLINGTON PAIR CURRENT AMPLIFIER

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – multimeter (1)	Collect hand tools (1)	4/2 = 2	
Hand tools	Use side cutters correctly (1)	Use wire stripper correctly (1)			2/2 = 1	
Preparation for insertion of components into breadboard.	Identify the pin layout of the transistor correctly (1)	Set supply voltage correctly at +9 V (1)			2/2=1	
Correct connection on breadboard – nodes and polarity	Connect 6 nodes correctly (6/2 = 3)	Polarity of TR1 and TR2 – correct (2)	Polarity of LED – correct (1)		6	
Circuit is working correct	1 transistor. Brightness of LED – dim (1)	2 transistors Brightness of LED – bright (1)			2	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in their places after work (1)			2/2=1	
Safety	Observing safety without being reminded (2)				2/2=1	
Facet sheet of Simulation 2B:					[14]	
Simulation 2A:					_____	(15)
Facet sheet of Simulation 2A:					_____	(15)
Simulation 2B:					_____	(6)
Facet sheet of Simulation 2B:					_____	(14)
TOTAL SIMULATION 2:						[50]

4.3 Simulation 3A: Monostable multivibrator using 555 IC

Name of learner: _____		Mark
Class: _____	Date Completed: _____	50
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

4.3.1 Purpose:

- To build the monostable multivibrator in FIGURE in 4.3.3 using a 555 IC.
- To justify the theory learned in class with the actual circuit.

4.3.2 Resources:

TOOLS/INSTRUMENTS	MATERIAL
Experiment board	1 x 555 IC
Voltmeter (multimeter)	2 x 10 k Ω resistors
DC power supply 5 V	1 x 1 k Ω resistor
Side cutters	2 x 470 Ω resistors
Long-nose pliers	1 x 220 μ F electrolytic capacitor 16 V
Wire stripper	1 x 220 μ F electrolytic capacitor 16 V
	1 x LED
	1 x push button/tactile switch
	Connecting wires

4.3.3 Procedure:

Build the circuit diagram in FIGURE 4.3.3 on your experiment board.
 After the teacher has checked the circuit, switch the power ON.
 Connect a multimeter to measure the voltage on pin 2.
 Connect a multimeter to measure the voltage across C₁.

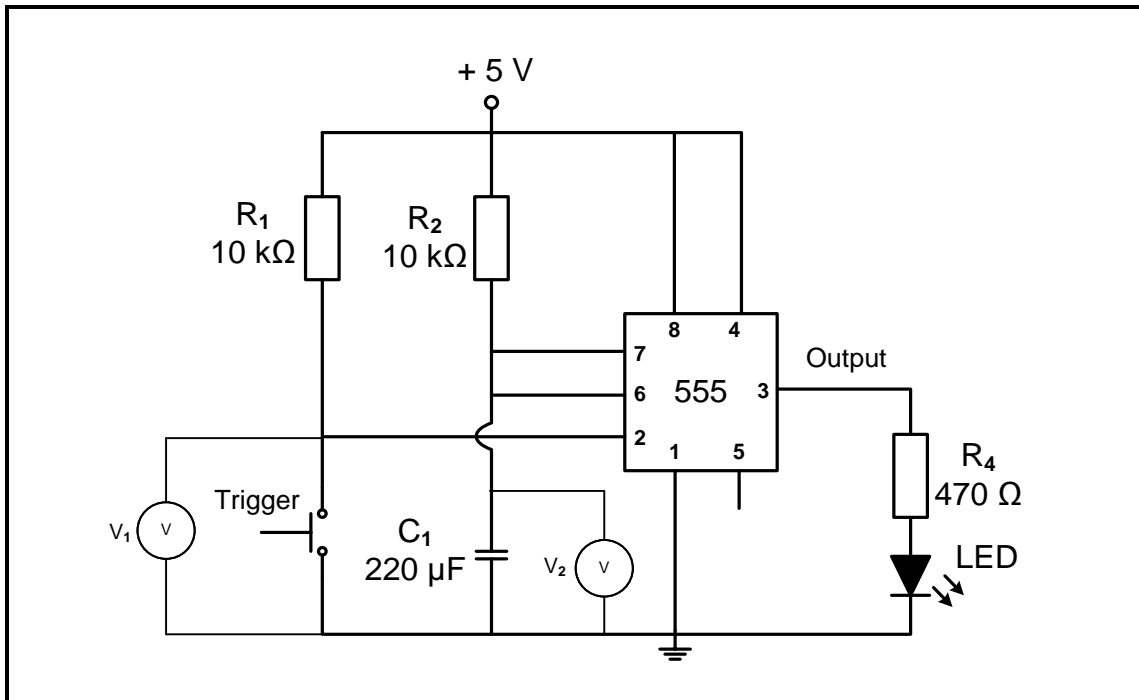


FIGURE 4.3.3: 555 MONOSTABLE MULTIVIBRATOR

- (a) Write down the voltage measured across pin 2.
Voltage on pin 2 $V_1 =$ _____ (1)
- (b) State the function of R_1 with reference to pin 2 and the output. (2)

- (c) Press the trigger input and observe what happens to the voltage measurement across the capacitor. Write down the voltage measured across C_1 just before the LED switches OFF (maximum charged voltage).
Voltage across C_1 . $V_2 =$ _____ (1)
- (d) Compare the voltage across C_1 with the supply voltage. (2)

- (e) Press the trigger input twice within a short time frame to simulate switch bounce. Write down your observation. (3)

- (f) Replace capacitor C_1 with a 100 μF capacitor. Switch ON the circuit, press the trigger input and observe. Write down you observation and give a reason why this happens. (3)

Simulation 3A: (12)

Simulation 3B: Inverting op-amp using 741 IC

4.3.4 Purpose:

To build the inverting amplifier circuit in FIGURE 4.3.6 using a 741 op-amp and to display the output waveforms on an oscilloscope. Investigate the effect of the R_F to R_{IN} ratio on the gain and the output of the amplifier.

4.3.5 Required resources:

TOOLS/INSTRUMENTS	MATERIAL
Function generator	1 x LM741 op-amp
Dual trace oscilloscope	1 x 100 kΩ resistors
+9 V 0 V -9 V DC power supply	1 x 50 kΩ variable resistor
Side cutters	Connecting wires
Wire stripper	
Calculator	

4.3.6 Procedure:

- Set the dual voltage power supply to +9 V/-9 V.
 - Set the function generator to deliver a 0,5 V peak 1 kHz sine wave.
 - Build the circuit in FIGURE 4.3.6 on your experiment board and connect it to the supply and input.
 - Connect channel 1 of the oscilloscope across the input to display at least TWO complete cycles.
 - Connect channel 2 of the oscilloscope across the output to display at least TWO complete cycles.
- (a) Build the circuit in FIGURE 4.3.6(a) on the experiment board with the variable resistor set to 10 kΩ.

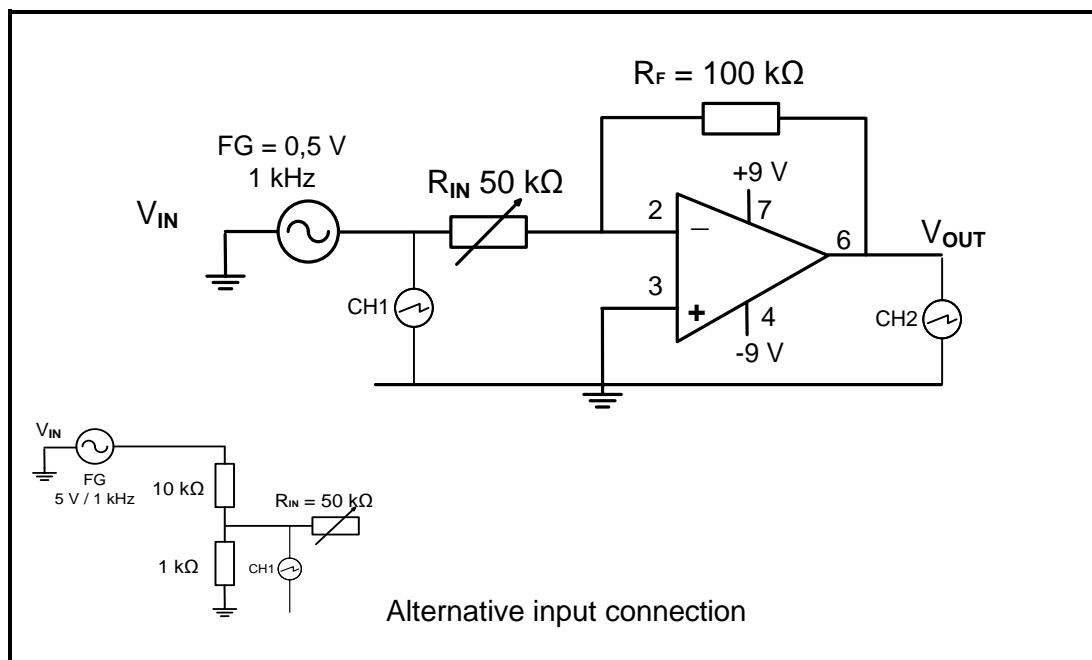
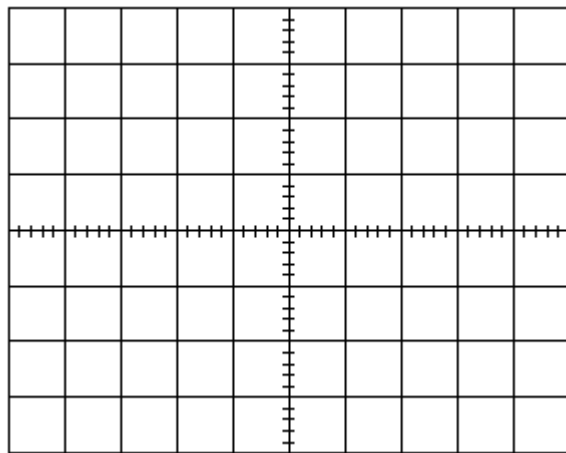


FIGURE 4.3.6(a): 741 INVERTING OP-AMP

- (b) Draw the input and output waveforms observed on the oscilloscope grid provided with the variable resistor set to 10 kΩ.



V/Div: _____ (Ch 1)

V/Div: _____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

(5)

- (c) Use the oscilloscope settings to determine the values of:

$V_{IN} =$ _____

(1)

$V_{OUT} =$ _____

(1)

- (d) Calculate the gain of the amplifier using the determined voltage values.

(3)

- (e) Set variable resistor R_{IN} to the following values and record the output voltage in TABLE 4.3.6(e).

(4)

R_{IN}	OUTPUT VOLTAGE
47 kΩ	
22 kΩ	
4,7 kΩ	
1 kΩ	

TABLE 4.3.6(e)

- (f) Compare the output voltages in TABLE 4.3.6(e) to the input voltage in (c) and write a conclusion.

(3)

Simulation 3B: (17)

Simulation 3C: Differentiator circuit using a 741 op-amp**4.3.7 Purpose:**

Wire the differentiator op-amp circuit In FIGURE 4.3.9 using a 741 IC and display the output waveforms on an oscilloscope. Investigate how the value of R_F and C_{IN} affects the shape of the output signal.

4.3.8 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Function generator Dual trace oscilloscope +9 V 0 -9 V DC power supply Side cutters Wire stripper	1 x 1 M Ω resistor 1 x 100 k Ω resistor 1 x 47 k Ω resistor 1 x 22 k Ω resistor (The feedback resistors can be replaced by a variable resistor within the prescribed range) 1 x 100 nF ceramic capacitor (104) 1 x LM 741 IC Connecting wires Alternatively a (102) or (103) ceramic capacitor may be used. Adjust the frequency accordingly.

4.3.9 Procedure:

- Set the dual voltage power supply to +9 V/-9 V.
- Set the function generator to deliver a 0,5 V peak 500 Hz triangular wave.
- Wire the circuit in FIGURE 4.3.9 on your experiment board and connect it to the supply and input.
- Connect channel 1 of the oscilloscope across the input to display at least TWO full cycles.
- Connect channel 2 of the oscilloscope across the output to display at least TWO full cycles.
- Vary R_F to 100 k Ω , 47 k Ω and 22 k Ω , measure and record the output.

(a) Wire the circuit in FIGURE 4.3.9 on the breadboard

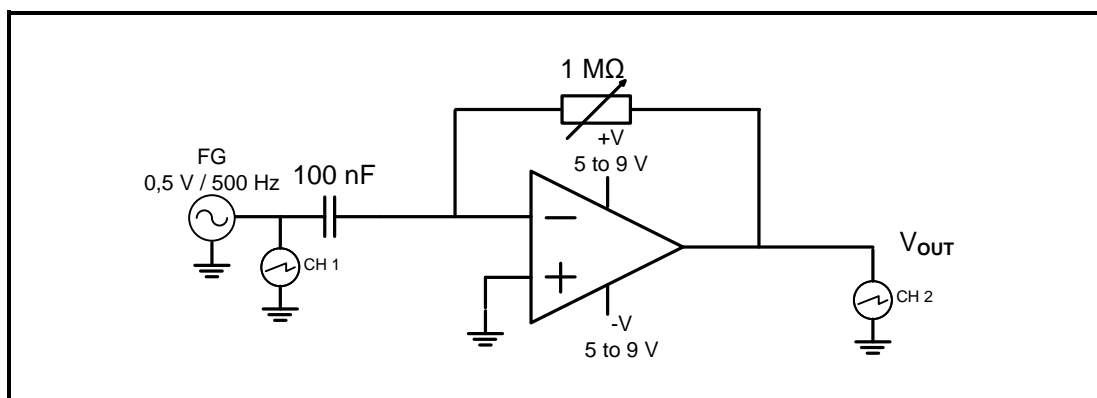
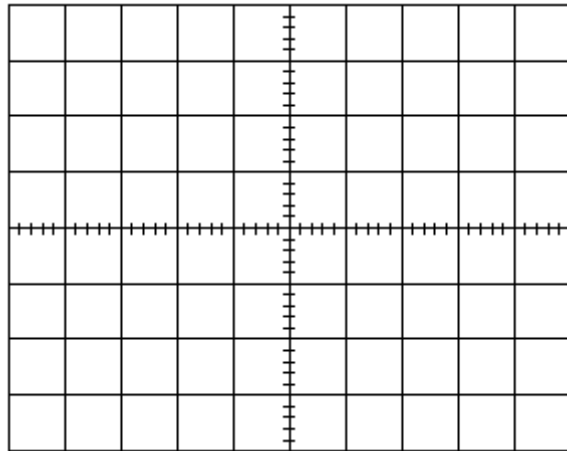


FIGURE 4.3.9: DIFFERENTIATOR CIRCUIT USING A 741 OP-AMP

(b) Draw the input and output waveforms on the oscilloscope grid provided.



V/Div: _____ (Ch 1)

V/Div: _____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

(5)

(c) Adjust the 1 MΩ resistor (R_F) to 100 kΩ. Switch on and observe.

(d) Adjust the 100 kΩ resistor (R_F) to 47 kΩ. Switch on and observe.

(e) Adjust the 47 kΩ resistor (R_F) to 22 kΩ. Switch on and observe.

4.3.10 CONCLUSION: Explain the effect different values of R_F and C_{IN} have on the output of the circuit.

(2)

Simulation 3C:

(7)

FACET SHEET FOR SIMULATIONS 3A, 3B AND 3C

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – multimeter (1)	Collect hand tools (1)	4/2 = 2	
Hand tools	Use side cutters correctly (1)	Use long-nose pliers correctly (1)	Use wire stripper correctly (1)		3/3 = 1	
Preparation for insertion of components into breadboard.	Check the pinout of the 555 IC (1)	Set supply voltage correctly at +5V for 555 IC (1)	Check the pinout of the 741 IC (1)	Set supply voltage correctly at +9 V 0 V -9 V for 741 IC (1)	4/2 = 2	
Correct connection on breadboard – nodes and polarity	Correct connection of 555 IC to supply (1)	Correct connection of 555 IC to input and output (2)	Correct connection of 741 IC to supply (1)	Correct connection of 741 IC to input and output (2)	6/2 = 3	
Circuit is working correctly	S ₁ is pressed - LED 1(red) ON (1)	LED stays on in relation with the RC time constant (1)	V _{out} is inverted with R _{IN} = 10 kΩ (1)	V _{out} is an inverted square wave when R _F = 1 MΩ and C _{IN} = 100 nF (1)	4	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in places after work (1)			2/2 = 1	
Safety	Observing safety without being reminded (1)				1	
Facet sheet for simulations 3A, 3B and 3C:					[14]	
Simulation 3A:					_____	(12)
Simulation 3B:					_____	(17)
Simulation 3C:					_____	(7)
Facet sheet 4: 741 of Simulation 3A, 3B and 3C:					_____	(14)
TOTAL Simulation 3:					[50]	

4.4 Simulation 4: Hartley oscillator

Name of learner: _____		Mark <hr style="width: 100px; margin: 0 auto;"/> 50
Class: _____	Date completed: _____	
Date Assessed: _____	Assessor Signature: _____	
Date Moderated: _____	Moderator Signature: _____	

4.4.1 Purpose:

Construction of the Hartley oscillator circuit using discrete components and displaying the input/output waveforms on the oscilloscope.

4.4.2 Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	1 x 2N2905 transistor
Analogue/Digital oscilloscope	1 x 470 KΩ resistor
Function generator	1 x 680 Ω resistor
Multimeter	1 x 2,2 KΩ resistor
Variable DC power supply	2 x 0,1 μF capacitor
Side cutters	1 x 47 μF capacitor
Wire stripper	1 x 0,1 μF capacitor
Long-nose pliers	2 x 47 nF capacitor
Connecting wire	1 x 0,47 μF capacitor
	1 x 10 mH inductor
	12 V DC supply

4.4.3 Procedure:

(a) Build the circuit in FIGURE 4.4.3 on the breadboard.

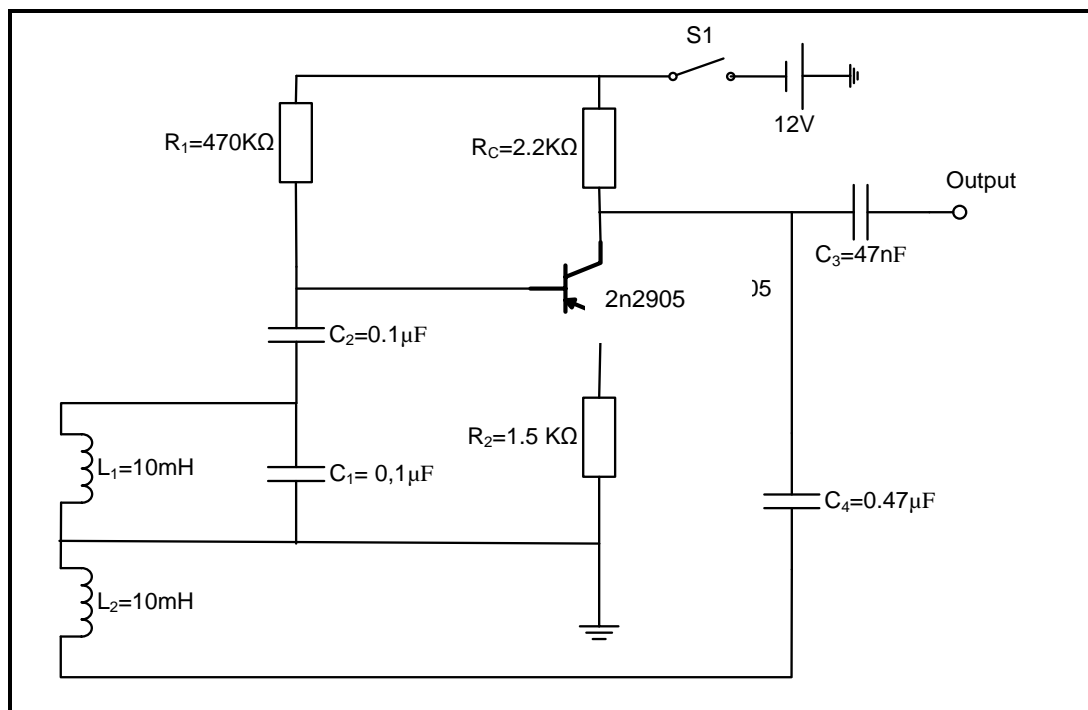
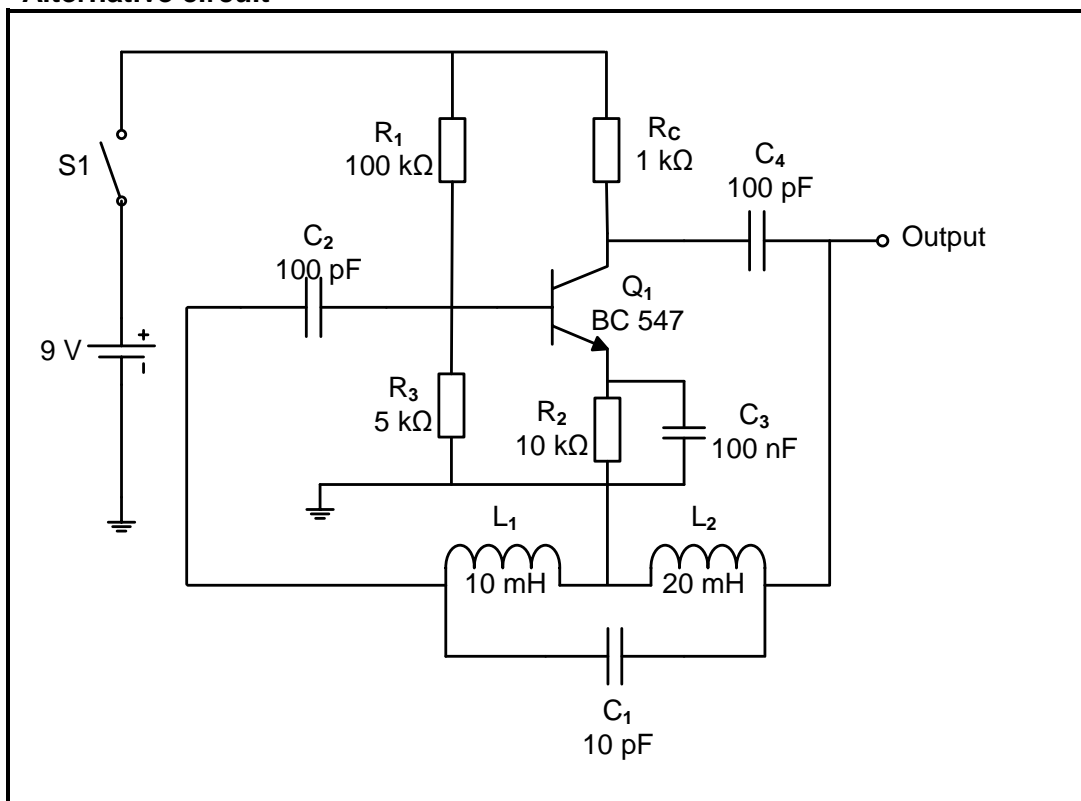
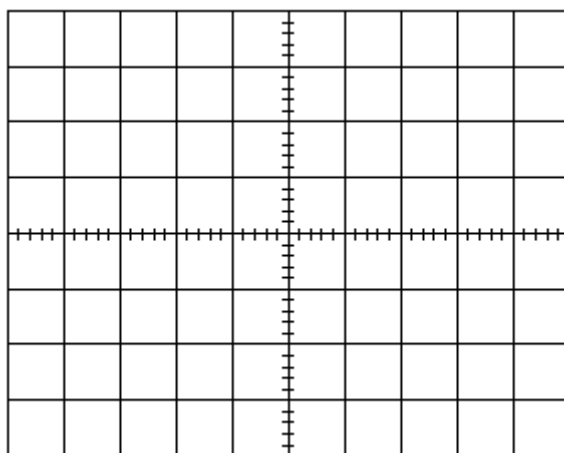


FIGURE 4.4.3: HARTLEY OSCILLATOR

Alternative circuit



(b) Switch ON the circuit. Draw the output of the oscillator on the grid provided.



V/Div: _____ (Ch 1)

T/Div: _____

NOTE: 1 mark for a correctly drawn waveform. 1 mark for each correct oscilloscope setting.

(3)

(c) Measure and record the following DC voltages:

- $V_{R1} =$ _____
- $V_{R2} =$ _____
- $V_{BE} =$ _____
- $V_{CE} =$ _____
- $V_{RC} =$ _____

- (2)
- (2)
- (2)
- (2)
- (2)

(d) Connect the oscilloscope, measure and record the resonant frequency _____ kHz. (2)

(e) Calculate the theoretical resonant frequency. (3)

(f) Replace capacitors C_1 and C_2 with $C_1 = 470 \text{ pF}$ and $C_2 = 1\,000 \text{ pF}$ respectively. Measure and record the oscillation frequency: (2)

(g) Calculate the theoretical resonant frequency of the new tank circuit. (3)

(h) Short out capacitor C_4 , observe and record the AC and DC measurements at the collector and record them.

AC = _____ (V) (2)

DC = _____ (V) (2)

(i) Explain the function of R_C in the circuit (3)


[30]

FACET SHEET FOR SIMULATION 4: HARTLEY OSCILLATOR

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – multimeter (1)	Collect hand tools (1)	4	
Hand tools	Use side cutters correctly (1)	Use long-nose pliers correctly (1)	Use wire stripper correctly (1)		3	
Preparation for insertion of components into breadboard	Refer to datasheet for pinout (1)	Set supply voltage correctly at 12 V (1)			2	
Correct connection on breadboard – nodes and polarity	Correct connection of transistor (2)	Correct polarity of supply (1)	Voltage measurement across components (3)		6	
Circuit is working correctly	Oscillation frequency at output sine wave (2)				2	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in the places after work (1)			2	
Safety	Observing safety without being reminded (1)				1	
Facet sheet of Simulation 4:					[20]	
Subtotal Simulation 4:					_____	(30)
Subtotal Facet sheet 4:					_____	(20)
TOTAL Simulation 4:						[50]

5. SECTION B – DESIGN AND MAKE

Design and Make Project	
Time:	January to August 2021
Learner Name:	_____
School:	_____
Class:	_____
Title/Type of Project:	_____


INSTRUCTIONS

- This section is **COMPULSORY** for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
 - SEVEN components
 - A variety of components (both active and passive)
 - PCB-making in some form
 - Soldering
 - An enclosure with a switch and protection
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST


NOTE: The learner **MUST** complete this checklist for the teacher **BEFORE** marking of that section takes place.

NO.	DESCRIPTION	TICK (☑)	
		NO	YES
Design and Make: Part 1			
1.	Circuit diagram drawn	<input type="checkbox"/>	<input type="checkbox"/>
2.	Circuit description filled in	<input type="checkbox"/>	<input type="checkbox"/>
3.	Component list completed	<input type="checkbox"/>	<input type="checkbox"/>
4.	Tools list for circuitry populated	<input type="checkbox"/>	<input type="checkbox"/>
5.	Measuring instrument list filled in	<input type="checkbox"/>	<input type="checkbox"/>
6.	Evidence of prototyping printed and pasted into the file	<input type="checkbox"/>	<input type="checkbox"/>
7.	Learner's own Veroboard/PCB planning/design printed and included in file	<input type="checkbox"/>	<input type="checkbox"/>
Design and Make: Part 2			
1.	Enclosure design completed and included in the file	<input type="checkbox"/>	<input type="checkbox"/>
2.	Unique name written down and on the enclosure	<input type="checkbox"/>	<input type="checkbox"/>
3.	Logo designed and placed on the enclosure	<input type="checkbox"/>	<input type="checkbox"/>
Miscellaneous			
1.	Enclosure included in the project	<input type="checkbox"/>	<input type="checkbox"/>
2.	Enclosure prepared and drilled according to the design	<input type="checkbox"/>	<input type="checkbox"/>
3.	Enclosure finished off and completed with name and logo	<input type="checkbox"/>	<input type="checkbox"/>
4.	PCB securely mounted in the enclosure using acceptable techniques	<input type="checkbox"/>	<input type="checkbox"/>
5.	Circuit inside the enclosure is accessible	<input type="checkbox"/>	<input type="checkbox"/>
6.	Internal wiring neat and ready for inspection	<input type="checkbox"/>	<input type="checkbox"/>
7.	File and project completed and ready for moderation at the workshop/room	<input type="checkbox"/>	<input type="checkbox"/>

5.1.6 **PCB design**

Design a printed circuit board layout for the circuit you are building.

Print it out and insert here.

A large, empty rectangular box with a black border, intended for the student to draw their PCB layout. The box is centered on the page and occupies most of the lower half of the document.

5.2 Assessment of the Design and Make Phase: Part 1

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *
Circuit Diagram (10)			
1.	The circuit diagram was drawn using EGD equipment.	1	
2.	The circuit diagram was drawn using CAD/any electronic design software.	1	
3.	The circuit diagram was drawn using correct symbols.	2	
4.	The circuit diagram has all labels – R1, C1, Tr1, etc.	2	
5.	The circuit diagram has all component values –100 Ω , 220 μF , etc.	2	
6.	The circuit diagram has a name/title.	1	
7.	The circuit diagram has a frame and title block. (EGD approach).	1	
Component List (3)			
8.	Labels correlate with circuit diagram.	1	
9.	Description and values correlate with circuit diagram.	1	
10.	Quantities are correct.	1	
Description of Operation (10)			
11.	Basic function of the circuit is described correctly.	2	
12.	All subcircuits in the circuit diagram and component list are included in the description.	3	
13.	Purposes of subcircuits in the circuit diagram are described correctly.	3	
14.	Learner used own interpretation and did not copy from another source verbatim.	1	
15.	Sources are acknowledged.	1	
Tools/Instrument List (2)			
16.	The tools/instrument list has been completed.	1	
17.	The tools/instruments listed all have a purpose for being used.	1	
Evidence of Prototyping on Breadboard (10)			
18.	Unique, original photos of the prototyping are included.	1	
19.	Unique, original photos include the learner name.	2	
20.	Photos are clear and in focus: All components are clearly identifiable.	2	
21.	Prototype is operational. No photo, no mark.	5	
PCB Design (15) (If a kit is used in this section = 0)			
22.	Printed Circuit Board design is included in the PAT file.	1	
23.	PCB design is made using a CAD approach.	5	
24.	Component overlay showing placement is included.	1	
25.	Components are labelled the same as in the circuit diagram.	1	
26.	The design is original and does not match any other learner's design.	2	
27.	Board layout (tracks/current flow) is functional and matches the original circuit diagram.	5	

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *
Circuit Board Manufacturing (70)			
28.	Circuit board is etched neatly according to the PCB design.	10*	
29.	The learner's name is etched onto the circuit design.	2	
30.	Holes are drilled neatly and are aligned in the middle of the pads on the PCB.	2	
31.	Mounting holes of the PCB are drilled symmetrically.	2	
32.	All burrs are removed.	2	
33.	The PCB is cut neatly/squarely and edges are filed neatly.	2	
34.	Axial and radial components are placed neatly and flush with the board.	2	
35.	Component orientation is aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2	
36.	Soldered components – leads are cut off, flush and neat on the solder side.	3	
37.	More than 60% of the solder joints are shiny (not dry joints).	5	
38.	Wire insulation is stripped to the correct length (no extra copper showing).	3	
39.	Wiring is long enough to allow for dismantling and inspection.	2	
40.	Wiring is wrapped neatly.	2	
41.	A power switch is included and fitted to the enclosure.	2	
42.	A fuse/Protection is included and fitted correctly where applicable.	2	
43.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2	
44.	Batteries are mounted using a battery housing/mounting bracket and battery clip (NO double-sided tape).	2	
45.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. (Switch is on – must go out when fuse is blown.)	3	
46.	The project is fully operational and commissioned/installed in the enclosure.	20	

TOTAL (PART 1 = 120 marks)	
---	--

NOTE: In projects where facets are not applicable, the projects should be marked and the totals adjusted accordingly.
--

5.3 Design and Make: Part 2**5.3.1 Enclosure design**

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.

5.3.2 Manufacture the enclosure neatly according to your design. You may use pre-cut panels from metal, wood and/or Perspex/Plexiglass. You must, however, construct/assemble these parts. Injection moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.

5.3.3 Choose a name for your device.
Write down the name of the device below.

5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.

[30]

5.4 Assessment of the Design-and-Make-Phase: Part 2

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *
Enclosure Design (10)			
1.	Enclosure design is included in first-angle orthographic projection.	2	
2.	Drawn design includes a title box and page border.	1	
3.	Isometric drawing included additionally.	2	
4.	Dimensions are included.	2	
5.	The name of the device is written in the PAT document.	1	
6.	The logo design and specification plate design is in the PAT document.	2	
Subtotal (10 marks max.)			
Enclosure Manufacturing (20)			
7.	Enclosure matches the design. – Dimensions and placement correlate.	1	
8.	Name of the device is attached on the enclosure.	1	
9.	The logo design is attached on the enclosure.	2	
10.	The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen printed/sublimation printed).	2	
11.	The enclosure is manufactured from scratch/pre-cut parts. Does NOT include: cardboard, paper, margarine container Does include: sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes	5	
12.	Holes/Cut-outs in the enclosure are made with the appropriate tools.	3	
13.	Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project.	2	
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2	
15.	The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.)	2	
Subtotal (20 marks max.)			

TOTAL (PART 2 = 30 marks)	
--	--

6. PROJECTS

Practical Project 6.1: 5-watt mini amplifier (portable speaker)

This micro-sized high-quality amplifier was originally designed to replace amplifiers in car radios where the original IC is no longer available. This does not limit the use to that application: use your imagination; there are a million other uses. Always use an adequate heat sink.

THE CIRCUIT

The TDA 2002 or TDA 2003 is used in a very straightforward audio amplifier configuration and only a few precautions must be taken when using it.

Firstly, because of the very high input impedance, the input connections must be screened cables and kept as short as possible to eliminate pickup of stray radio frequency and other interference. Secondly, the fact that the PC board is so small, limits the amount of decoupling capacitance (C5) that can be provided on the board. If the supply does not have at least a few hundred microfarads smoothing, then the amplifier could go into oscillation, and that means you have to place, say 1 000 μF 16 V capacitor over the supply voltage

Tips on construction

No problems should be experienced when assembling this amplifier. Just check for the polarity of the electrolytic capacitors and make sure that the soldering is done properly. Care must also be taken when connecting the power to the PC board.

IF THE POLARITY IS REVERSED, THE IC WILL BE DESTROYED!

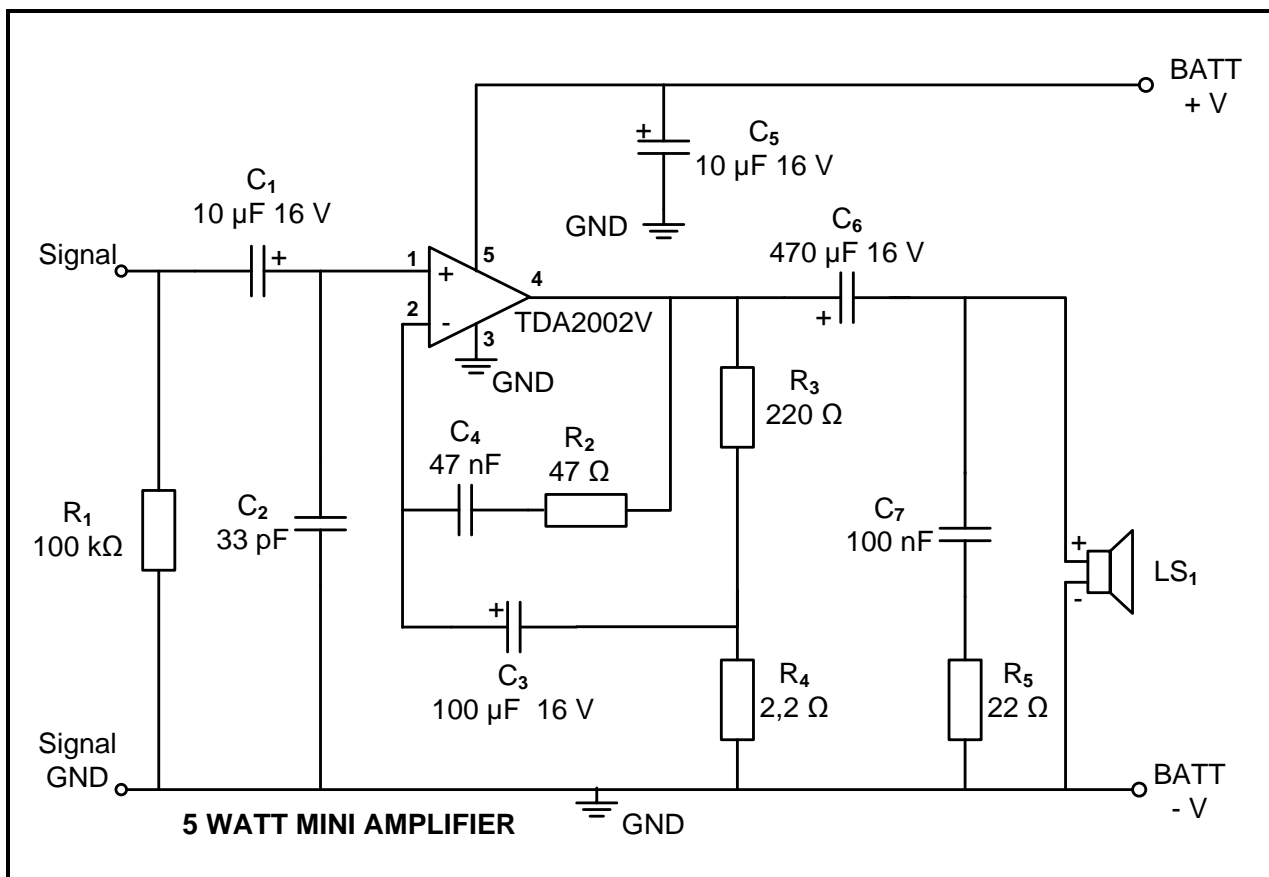
COMPONENT LIST

R ₁	Can be replaced with a 100 K pre-set if required					
R ₁	100 K 1/4 W resistor	Brown	Black	Yellow	Gold	1
R ₂	47 ohm 1/4 W resistor	Yellow	Violet	Black	Gold	1
R ₃	220 ohm 1/4 W resistor	Red	Red	Brown	Gold	1
R ₄	2,2 ohm 1/4 W resistor		Red	Red	Gold	1
R ₅	22 ohm 1/4 W resistor	Red	Red	Black	Gold	1
C ₁	10 μF 16 V electrolytic radial capacitor					1
C ₂	33 pF non-polarized ceramic capacitor					1
C ₃	100 μF 16 V electrolytic radial capacitor					1
C ₄	47 nF non-polarized capacitor (473, 0,047 μF)					1
C ₅	10 μF 16 V electrolytic radial capacitor					1
C ₆	470 μF 16 V electrolytic radial capacitor					1
C ₇	100 nF non-polarized capacitor (104, 0,1 μF)					1
IC ₁	TDA 2002 OR TDA 2003 sound IC					1
PP ₃	9 V battery clip					1
	10 cm mono-screened cable for signal IN connection					1
PCB	EFK # 1002					1

Required resources:

TOOLS/INSTRUMENTS	MATERIALS
Oscilloscope (analogue/digital)	Side cutters
Analogue/Digital trainer with dual power supply	Wire strippers
Multimeter	Soldering iron
PCB etching tank or similar	Helping hands
	Solder sucker

Circuit Diagram



Practical Project 6.2: (Electronics): Dual voltage power supply

This project uses a centre-tapped transformer. The recommended rating of the transformer is 240 V to 18-0-18 V.

NOTE: Sometimes the transformer you purchase outputs more than the specified value, so be careful while choosing the transformer.

Capacitors C1 and C2 act as the smoothing capacitor; this is to even out any fluctuation in voltage. You can also add a bypass capacitor after the C1 and C2 to remove any AC noise which is not shown in the circuit. Besides the two voltage regulators, the 7812 gives positive 12 V and 7912 gives you negative 12 V. Other variants of voltage regulator ICs can also be used.

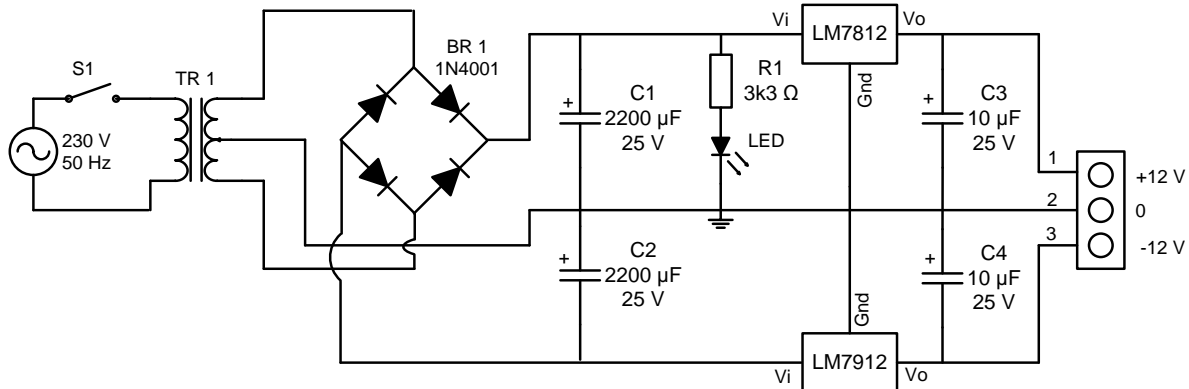
NOTE: 78xx gives the positive output and 79xx gives the negative output.

Capacitors C3 and C4 are used as the bypass capacitor to remove the AC noise and give a pure and cleaner DC Signal.

Required resources:

TOOLS	MATERIALS	
Multimeter	1 x transformer 240 to 15-0-15 volt	1 x 7812 voltage regulator IC
Side cutters	- 4 x 1N4001	1 x 7912 voltage regulator IC
Wire strippers	2 x 2 200 uF/25 v	1x toggle switch
Soldering iron	2 x 10 uF/25 v	1 x in-line fuse and holder
Helping hands	1 x 3,3 kΩ	1 m mains supply cable
PCB etching tank or similar	1 x red LED	1 x 3 pin plug
Solder sucker	2 x heat sink	1 x PCB
	2 x 3 pin terminal block	

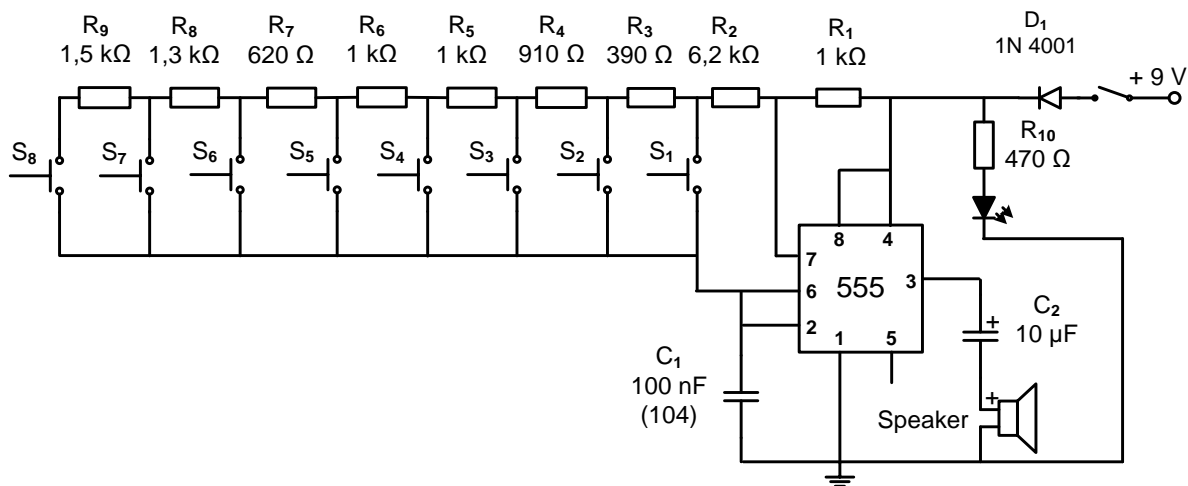
Circuit diagram:



Practical Project 6.3: Electronic piano

The electronic piano uses an astable mode of a common 555 timer integrated circuit to produce a tone that drives the speaker (piezo buzzer).

Each musical note has a specific frequency. The frequency produced by the 555 timer in astable mode relies on the values of capacitor (C_1) and two resistances (R_1 and a combination of R_2 to R_9). The resistance of R_2 to R_9 will vary depending on which push button is pressed.



TOOL	MATERIALS	
Multimeter	9 V battery and battery clip	470 Ω resistor
Side cutters	SPST switch	LED red x 1
Long-nose plier	Fuse and fuse holder	100 nF ceramic capacitor (104)
Wire strippers	1N 4001 diode	10 μF electrolytic capacitor
Soldering iron	1 kΩ resistor x 3	16V
Solder sucker	390 Ω resistor	IC NE555
Helping hands	910 Ω resistor	Speaker 8 Ω/buzzer
PCB etching tank or similar	620 Ω resistor	PCB
	1k3 Ω resistor	Solder
	1k5 Ω resistor	Etching chemicals

NOTE:

All circuits MUST include an ON/OFF switch with a ON indicator and fuse protection.

7. CONCLUSION

On completion of the practical assessment task learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.