

basic education

Department: Basic Education **REPUBLIC OF SOUTH AFRICA**

ELECTRICAL TECHNOLOGY (DIGITAL ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS

GRADE 12

2021

These guidelines consist of 43 pages.

TABLE OF CONTENTS

1.	PA INTRODUCTION/BACKGROUND	AGE 3
2.	TEACHER GUIDELINES2.1How to administer PATs2.2How to mark/assess PATs2.3PAT Programme of Assessment (PAT PoA)2.4Moderation of PATs2.5Absence/Non-submission of tasks2.6Simulations2.7Projects2.8Working Mark Sheet	4 4 5 6 7 7 8
3.	LEARNER GUIDELINES3.1PAT 2021 cover page3.2Instructions to learners3.2Declaration of Authenticity (Compulsory)	9 9 10 10
4.	 SIMULATIONS 4.1 Simulation 1A: Monostable multivibrators using a 555 IC Facet Sheet of Simulation 1A: Monostable vibrator Simulation 1B: Astable multivibrator Rubric of Simulation 1B 4.2 Simulation 2A: 741 inverting op-amp Simulation 2B: Differentiator amplifier circuit using the 741 op-amp Facet sheet for Simulation 2A and 2B: 741 inverting op-amp and differentiator 4.3 Simulation 3: Connecting a 7-segment display to a 4-bit BCD 7-segment driver Facet sheet for Simulation 3: Connecting a 7-segment display to a 4-bit BCD 7-segment driver 4.4 Simulation 4A: RS latch circuit Rubric for Simulation 4A Simulation 4B: PICAXE Facet sheet for Simulation 4B: PICAXE flowchart 	11 14 15 17 18 21 23 24 26 28 30 31 32
5.	 SECTION B: DESIGN AND MAKE 5.1 Design and make: Part 1 5.2 Assessment of the design and make phase: Part 1 5.3 Design and make: Part 2 5.4 Assessment of design and make phase: Part 2 PROJECTS 	33 34 37 39 40 41
o. 7.	6.1 Practical project 6.1: Traffic light 6.2 Practical project 6.2: Two-digit object/Product counter CONCLUSION	41 42 43
1.		43

1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- AGRICULTURE: Agricultural Management Practices, Agricultural Technology
- ARTS: Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- SCIENCES: Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- SERVICES: Consumer Studies, Hospitality Studies, Tourism
- TECHNOLOGY: Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps needs to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for power systems.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2021 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
 - Enclosure:
 - The file must include a design.
 - The enclosure and the design must match.
 - No cardboard boxes are allowed.
 - Plastic wooden and metal enclosures are acceptable.
 - Enclosures that are manufactured and/or assembled by the learners are preferred.
 - The enclosure should be accessible for scrutiny inside.
 - Lids that are secured are preferred.

- Circuit board:
 - The file should include the PCB design.
 - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
 - Switches, potentiometers, connectors and other items must be mounted.
 - Wiring must be neat and bound/wrapped.
 - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
- Logo and name:
 - The file should contain the logo and name design and specification plate.
 - Logo, specification plate and name must be prominent on the enclosure.
 - The logo/specification plate must be affixed in a permanent manner painted, glued or stuck on with vinyl

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the FIRST THREE TERMS and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must not be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a **working model and model answer file** that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. **No re-assessment will be done once the facet sheets have been completed** and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

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2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2021	Teacher – Builds the models and works out the model answers for the simulations for 2021. Identifies shortages in tools, equipment and consumable items for simulations that must be procured in 2021
		SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2021	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
January 2021	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to
February 2021	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2021	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
April–June 2021	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate Simulation 1 10% of learners' work is moderated
April–June 2021	PAT project – learners continue with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2021 July–August	PAT intervention Moderation of	Learners that are behind on the PAT are required to complete the project during this holiday. District subject facilitator/subject specialist will visit the school and
2021	Simulation 2	moderate Simulations 2 – different learners from the previous term 10% of learners' work is moderated
July–August 2021	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed
September– October 2021	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly

2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulations 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. Both simulations will be moderated.
- The teacher is required to build an exemplar model for each project type chosen for the school.
- This model must be on display during moderation.
- The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).
- Level 5 assessments must exceed the model of the teacher in skill and finishing.
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.
- The moderator will randomly select no fewer than **two projects** (not simulations) and the learners involved will have to explain how the project was manufactured.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of Tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

7

2.6 Simulations

Simulations are circuits, experiments and tests/tasks which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who make use of simulation programs on a computer may use it for the learners to practice on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

- STEP 1: The teacher will choose simulations from the provided examples.
- STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items are lost/damaged very easily when learners work with them.
- STEP 3: Contact three different electronics component suppliers for comparative quotations.
- STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
- STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
- STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/ resource availability.

Teachers are required to develop a set of model answers in the teacher's file.

Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on proven circuits provided from schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects are varied in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They MUST redraw these circuits in their file correctly.

The description of the operation of the circuits is NOT complete. It is required of learners to interrogate the function of the components in the provided circuit. They should elaborate on the purpose of components in the circuit. It is recommended that those learners investigate similar circuits available on the internet and in the school library or workshop reference books.

2.8

Working mark sheet (A working Excel file is provided with this PAT)

PAT mark sheet	Term 1	Term 2	Pro	oject		00	ark
No. Name of Learner	Simulation 1 50	Simulation 2 50	Design and Make Part 1 120	Design and Make Part 2 30	Total = Term 1 + Term 2 + Project 250	Mark out of 100	Moderated Mark
1							2
2							
3							
4							
5							
6							
7							
8							
9							
10							
11 12							
13							
14							
15							
Total							
Average							

Teacher Name:	Principal Name:	Moderator Name:
Signature:	Signature:	Signature:
Date:	Date:	Date:

3. LEARNER GUIDELINES

PAT 2021 cover page (Place this page at the front of the PAT.)

Department of Basic Education
Grade 12
CAPS for Technical High Schools
Practical Assessment Task – Electrical Technology
Time allowed: Terms 1–3 (2021)
Learner Name:

Class:

School:

Specialisation: DIGITAL ELECTRONICS

Complete TWO simulations.

Project (Write the name of the project): _____

Evidence of moderation:

NOTE:

When the learner evidence (LE) selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation 1	50		
Simulation 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
Total	250		

3.1 Instructions to learner

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work and co-operative work is not allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain **2** simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO digits. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and can be in colour or greyscale. Scanned photos and photocopies are allowed.
- This document must be placed inside your PAT file together with the other evidence.
- Learners with identical photos will be penalised and receive zero for that section

3.2 Declaration of Authenticity (COMPULSORY)

Declaration: I ______ herewith declare that the work represented in this evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

Signature of learner

Date

4. SIMULATIONS

4.1 Simulation 1A: Monostable multivibrators using a 555 IC

Name of learner:				
Class:	Date Completed:	Mark	50	
Date Assessed:	Assessor Signatu	ıre:		
Date Moderated:	Moderator Signat	ure:		

4.1.1 Purpose:

- To study a monostable multivibrator using a 555 IC.
- To build a bistable multivibrator with the 555 IC.
- To compare the theory learned in class with the actual circuit •

4.1.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Breadboard Voltmeter (multimeter) DC power supply 5 V Side cutters Long-nose pliers Wire stripper	1 x 555 IC 2 x 10 kΩ resistors 1 x 1 kΩ resistor 2 x 470 Ω resistors 1 x 220 μ F electrolytic capacitor 16 V 1 x LED 1 x push button/tactile switch
	Connecting wires

4.1.3 **Procedure:**

Build the circuit diagram in FIGURE 4.1.3 on your breadboard. After the teacher has checked the circuit, switch the power ON. Connect a multimeter to measure the voltage on pin 2. Connect a multimeter to measure the voltage across C1.

(2)

(2)

(2)

(2)

(4)

+ 5 V

R₁ R_2 10 kΩ 10 kΩ 8 4 7 Output 555 3 6 2 1 5 R₄ 470 Ω Trigger C_1 LED 220 µF V2 v FIGURE 4.1.3: MONOSTABLE MULTIVIBRATOR (a) Write down the voltage measured across pin 2 Voltage on pin 2 V₁ = (b) State the function of R_1 with reference to pin 2 and the output. Press switch S₁ and observe what happens to the voltage measurement across the capacitor. Write down the voltage measured across C1 just before the LED switches OFF (maximum charged voltage). Voltage across C_1 . $V_2 =$ (d) Compare the voltage across C_1 to the supply voltage. (e) Press switch S_1 twice within a short time frame to simulate switch bounce. Write down your observation.

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(c)

(f) Replace capacitor C_1 with a 100 μ F capacitor. Switch ON the circuit, press switch S_1 and observe. Write down your observation and give a reason why this happens.

Simulation 1A: [16]

FACET SHEET OF SIMULATION 1A: MONOSTABLE MULTIVIBRATOR

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – multimeter (1)	Collect hand tools (1)	4	
Hand tools	Use side cutters correctly (1)	Use long-nose pliers correctly (1)	Use wire stripper correctly (1)		1	
Preparation for insertion of components into breadboard.	Check the pin out of the 555 IC on the relevant data sheet (1)	Set supply voltage correctly at +5 V (1)			1	
Correct connection on breadboard – nodes and polarity	Correct connection of 555 IC to the supply (2)	Polarity and connection of switches – correct (2)	Polarity LED – correct (1)		5	
Circuit is working correctly	S1 is pressed – LED 1(red) ON (1)	LED stays on in relation to the RC time constant (1)			2	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in places after work (1)			2	
Safety	Observing safety before being reminded (2)	Observing safety after being reminded (1)			2	
			Facet sheet of	of Simulation 1A:	[17]	

Simulation 1B: Astable multivibrators

4.1.4 **Purpose:**

Build an electronic piano (astable multivibrator) using the 555 IC in FIGURE 4.1.6 on a breadboard and display the output waveforms on an oscilloscope.

4.1.5 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	1 x 555 timer IC
Analogue/Digital oscilloscope	1 x 100 nF capacitor
Function generator	1 x 10 µF (electrolytic capacitor 25 V)
Variable DC power supply	5 x 1 kΩ resistor
Side cutters	1 x 10 kΩ potentiometer
Wire stripper	1 x 8 Ω speaker/buzzer
	5 x push buttons
	Connecting wires

4.1.6 **Procedure:**

Build the circuit in FIGURE 4.1.6 on the breadboard.
 Connect channel 1 of the oscilloscope to pin 3 of the 555 IC.
 Switch ON the circuit, press the push buttons (one at a time) and observe.
 Answer the questions that follow.



FIGURE 4.1.6: ASTABLE MULTIVIBRATOR

(2)

16 NSC

(b) Press push button S_1 and draw the output wave observed on the oscilloscope grid provided. Set the oscilloscope to display at least FOUR complete cycles.

		-				V/Div: (Ch 1)
		-	-			T/Div:
 	 	+++++	+++++	 	 	NOTE: 1 mark for the correctly drawn waveform. 1 mark for the oscilloscope
		-				settings.

(c) Make use of the oscilloscope settings and determine the frequency of the signal.

(d) Press push button S_5 and draw the output wave observed on the oscilloscope grid provided. Do NOT adjust the time per division setting.

						V/Div: (Ch 1)	
		-				T/Div:	
 	 	+++++	• • • • • •	 	 	NOTE: 1 mark for the correctly drawn waveform. 1 mark for the oscilloscope	
		-				settings.	
							(2)

(e) Make use of the oscilloscope settings and determine the frequency of the signal.

Frequency when S_5 is pressed		(2)
	_	

(f) Press each of the push buttons and observe.Explain why there is a difference in the output for each push button. (3)

Simulation 1B: [11]

RUBRIC FOR SIMULATION 1B

0	1	2	LEARNER MARK
Learner was not able to connect the circuit correctly	Learner was able to connect a part of the circuit correctly without assistance	Learner was able to connect the whole circuit correctly without assistance	
The learner was not able to display the output wave on the oscilloscope	The learner was able to set the oscilloscope and managed to get the output wave after the assistance from the teacher	The learner was able to set the oscilloscope and managed to get the output wave without the assistance of the teacher	
Learner did not do any housekeeping duties	Learner did housekeeping after being reminded	Learner did housekeeping without being reminded	

(6)

Simulation 1A: (16)

Facet sheet of Simulation 1A: (17)

Simulation 1B: (11)

Rubric of Simulation 1B: (6)

TOTAL SIMULATION 1: [50]

4.2 Simulation 2A: 741 inverting op-amp

Name of learner:				
Class:	_ Date completed:	Mark	50	
Date Assessed:	Asses	ssor Signature:		
Date Moderated:	Mode	rator Signature:		

4.2.1 **Purpose:**

Build the inverting amplifier circuit in FIGURE 4.2.3 and display the output waveforms on the oscilloscope. Investigate the effect of R_F to R_{IN} ratio on the gain and the output of the amplifier.

4.2.2 **Required Resources:**

TOOLS/INSTRUMENTS	MATERIALS
Function generator	1 x LM741 op-amp
Dual trace oscilloscope	1 x 100 kΩ resistor
+9 V 0 V–9 V DC power supply	1 x 10 k Ω resistor
Side cutters	1 x 1 k Ω resistor
Wire stripper	Connecting wires
Calculator	Ŭ

4.2.3 **Procedure:**

Set the dual voltage power supply to +9 V/-9 V.

Set the function generator to deliver a 0,5 V peak 1 kHz sine wave.

Connect the circuit in FIGURE 4.2.3 on the breadboard and connect it to the supply.

Connect channel 1 of the oscilloscope across the input to display at least TWO complete cycles.

Connect channel 2 of the oscilloscope across the output to display at least TWO complete cycles.

Answer the questions that follow.

Connect the circuit in FIGURE 4.2.3 on the breadboard. (a)



FIGURE 4.2.3: 741 INVERTING OP-AMP

(b) Draw the input and output waveforms observed on the oscilloscope grid provided.

	ŧ		V/Div: (Ch 1)	
			V/Div: (Ch 2)	
			T/Div:	
+++++++++++++++++++++++++++++++++++++++		 ••••		
			NOTE: 1 mark for each correctly drawn waveform. 1 mark for the	
			oscilloscope settings.	
			(3	3)

Use the oscilloscope settings and determine the values of: (C)

V_{IN} = (1) (1)

- V_{OUT} =
- Calculate the gain of the amplifier. (d)

(3)

(e) Replace the R_{IN} 10 k Ω resistor with the following resistors and write down the value of the output voltage. (4)

R _{IN}	OUTPUT VOLTAGE							
47 kΩ								
22 kΩ								
4,7 kΩ								
1 kΩ								
T	TABLE 4.2.3(e)							

(f) Compare the output voltages in TABLE 4.2.3(e) to the output voltage in (c) and write a conclusion. (4)



Simulation 2B: Differentiator amplifier circuit using the 741 op-amp

4.2.4 **Purpose:**

Connect a differentiator op-amp circuit using a 741 IC and display the output waveforms on an oscilloscope. Investigate how the value of R_F and C_{IN} affects the shape of the output signal.

4.2.5 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Function generator Dual trace oscilloscope +9 V 0–9 V DC power supply Side cutters Wire stripper	 1 x 1 MΩ resistor 1 x 100 kΩ resistor 1 x 47 kΩ resistor 1 x 22 kΩ resistor 1 x 100 nF ceramic capacitor (104) 1 x 100 nF ceramic capacitor (104) 1 x LM 741 IC Connecting wires Alternatively a (102) or (103) ceramic capacitor may be used. Adjust the frequency accordingly.

4.2.6 **Procedure:**

Set the dual voltage power supply to +9 V/-9 V.

Set the function generator to deliver a 0,5 V peak 500 Hz triangular wave.

Connect the circuit in FIGURE 4.2.6 on your breadboard and connect it to the supply and input.

Connect channel 1 of the oscilloscope across the input to display at least TWO full cycles.

Connect channel 2 of the oscilloscope across the output to display at least TWO full cycles.

(a) Connect the circuit as in FIGURE 4.2.6 on the breadboard.



FIGURE 4.2.6: DIFFERENTIATOR AMPLIFIER CIRCUIT

(b) Draw the input and output waveforms on the oscilloscope grid provided.

						V/Div: (Ch 1)				
						V/Div: (Ch 2)				
						T/Div:				
 	 	+++++		 	++++	 NOTE: 1 mark for each correctly drawn waveform.				
		-	<u> </u>			1 mark for the oscilloscope settings.				
			<u> </u>							

- (c) Replace the 1 M Ω resistor (R_F) with a 100 k Ω resistor. Switch on and observe.
- (d) Replace the 100 k Ω resistor with a 47 k Ω resistor. Switch on and observe.
- (e) Replace the 47 k Ω resistor with a 22 k Ω resistor. Switch on and observe. Draw the input and output waveforms on the oscilloscope grid provided.

						V/Div: (Ch 1)				
						V/Div: (Ch 2)				
						T/Div:				
 	 	+++++	- 	 	 ++++	NOTE: 1 mark for each				
						correctly drawn waveform. 1 mark for the oscilloscope settings.				
			<u> </u>			-				

4.2.7 Write a conclusion on why the values of R_F and C_{IN} affect the output of the circuit.

(3)

(3)

(4)

Simulation 2B: [10]

FACET SHEET FOR SIMULATIONS 2A AND 2B: 741 INVERTING OP-AMP AND DIFFERENTIATOR

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the	Identify components	Collect PSU/	Collect instruments –	Collect hand	4	
simulation	correctly (1)	mini trainer (1)	multimeter (1)	tools (1)		
Hand tools	Use side cutters correctly (1)	Use long-nose pliers correctly (1)	Use wire stripper correctly (1)		3	
Preparation for insertion			conectly (1)		2	
-	Check the pinout of	Set supply voltage			Z	
of components into	the 741 IC (1)	correctly at $+9 \vee 0 \vee -9$				
breadboard		V (1)			•	
Correct connection on	Correct connection	Correct connection of	Correct connection of		6	
breadboard – nodes and	of 741 IC to supply	R_{IN} and R_F to 741 IC	R_F and C_{IN} to 741 IC			
polarity	(2)	(2)	(2)			
Circuit is working	V _{out} is inverted with	V _{out} is an inverted	Correctly setting up the		4	
correctly	R _{IN} = 10 kΩ (1)	square wave when	oscilloscope to display			
		$R_F = 1 M\Omega$ and	at least TWO full cycles			
		C _{IN} = 100 nF (1)	(2)			
Housekeeping	Cleaning the	Return tools to places			2	
	working area after	after work				
	the experiment (1)	(1)				
Safety	Observing safety	Observing safety after			3	
	before being	being reminded				
	reminded (3)	(2)				
			Facet sheet for Simulati	ons 2A and 2B:	[24]	

- ____ Simulation 2A: (16) Simulation 2B: (10) (24)
- Facet sheet of Simulation 2A and 2B:
 - **TOTAL Simulation 2:** [50]

23 NSC Simulation 3: Connecting a 7-segment display to a 4-bit BCD 7-segment driver

Name of learner:				
Class:	Date Completed:	Mark	50	
Date Assessed:	Assesso	r Signature:		
Date Moderated:	Moderato	or Signature:		

Activity 3A

4.3

4.3.1 **Purpose:**

Connect a simple circuit to connect a 7-segment display to a 4-bit BCD 7-segment display driver.

4.3.2 **Required Resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer	4 x LEDs
Breadboard	4 x 390 Ω resistors
Variable DC power supply	7 x 1k resistors
Side cutters	CD4511 IC
Breadboard wire	CD4518B IC
	5 x SPST switches
	7-segment display

4.3.3 **Procedure:**

Connect the circuit as in the circuit given below:



An alternative circuit can be used

FACET SHEET FOR SIMULATION 3: CONNECT A 7-SEGMENT DISPLAY TO A 4-BIT BCD 7-SEGMENT DRIVER

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – oscilloscope (1)	Collect hand tools (1)	4	
Hand tools	Use side cutters correctly (1)	Use wire stripper correctly (1)			2/2 = 1	
Preparation for insertion of components into breadboard.	Check the datasheet on the ICs (1)	Set supply voltage correct at +9 V (1)			2	
Correct connection on breadboard – nodes and polarity	8 nodes for correct connection of CB4518B IC (8/8 = 8)	20 nodes for correct connection of CD4511 IC and the 7-segment display (20/.75 = 15)			23	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back to the places after work (1)			2	
Safety	Observing safety before being reminded (2)	Observing safety after being reminded (1)			3	
			Facet sheet for	Simulation 3:	[35]	

26 NSC

Activity 3B

Conduct the following steps and answer the questions in the space provided.

STEP	IC CD4185 GIVEN CODE	7-SEGMENT DISPLAY	
(a)	Which number is displayed on the 7-segment display if the binary number 0111 is illuminated on the output LED's of the counter?		(3)
(b)	Which number is displayed on the 7-segment display if the binary number 1000 is illuminated on the output LED's of the counter?		(3)
(C)	Which number is displayed on the 7-segment display if the binary number 1001 is illuminated on the output LED's of the counter?		(3)
(d)	Which number is displayed on the 7-segment display if the binary number 0011 is illuminated on the output LED's of the counter?		(3)
(e)	Which number is displayed on the 7-segment display if the binary number 0101 is illuminated on the output LED's of the counter?		(3)

[15]

Activity 3A: Activity 3B: (35)

(15)

Total Simulation 3: [50]

Simulation 4A: RS latch circuit and PICAXE 4.4

Name of learner:			! !	
Class:	Date completed:	Mark	50	
Date Assessed:		Assessor Signature:		
Date Moderated:		Moderator Signature:		

4.4.1 Purpose:

To demonstrate the operation of the RS latching practically.

4.4.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Breadboard	74L500 IC
Voltmeter	Toggle switches x 2
Dual power supply 9 V 0–9 V	1 kΩ resistor x 2
Dual Power Supply 5 V 0–5 V	220 Ω resistor x 2
Side cutters	1 x red and 1 x green LED
Wire stripper	Connecting wires

4.4.3 **Circuit diagram**

Connect the circuit as in FIGURE 4.3.3 on the breadboard. After you switch on the circuit, press the set switch. You will be assessed with the rubric on the next page.



FIGURE 4.3.3: CIRCUIT DIAGRAM OF AN RS LATCH CIRCUIT

NS

4.4.4 **Procedure:**

- Apply logic 0 to S input, and observe the Q output.
- Return the S input to logic 1 and observe the Q output.
- Apply logic 0 to S and R, and observe the Q output.
- Apply logic 1 to S and R, observe the Q output.

RUBRIC FOR SIMULATION 4A:

	LEVEL DESCRIPTOR				
1	2	3	5	OBTAINED	
The learner could not identify the correct components	The learner identified the correct components but could not build the circuit on the breadboard	The learner did build the circuit after assistance of the teacher	The learner managed to identify the correct components and build the circuit without the assistance of the teacher		
The learner could not use the measuring instruments	The learner managed to calibrate instruments after assistance of the teacher	The learner managed to use the instruments and managed to get ONE reading required after the assistance of the teacher	The learner managed to use the instruments and managed to get ALL the readings required without the assistance of the teacher		

4.4.5 **Observations:**

- (a) Press the reset and set switches. Write down your observation.
- (3)

(3)

(10)

- (b) Press both reset and set switches simultaneously. Write down your observation.
- 4.4.6 Complete the truth table based on the operation of the circuit you have constructed.

INPUTS		OUTPUTS	
S	R	Q	\overline{Q}
0	0		
0	1		
1	0		
1	1		

(4)

4.4.7 Housekeeping:

When you have obtained all the measurements and the teacher has validated all your answer you must tidy up your workplace as part of the safety in the workshop. You will be assessed on housekeeping with the rubric below.

RUBRIC

	LEVEL DESCRIPTOR				
0	2	3	5	OBTAINED	
The candidate did not do any housekeeping.	The candidate did do house- keeping after the teacher reminded the candidate.	The candidate did do housekeeping, but only tidied up his/her own workplace and did not help with the cleaning of the rest of the workshop.	The candidate did house- keeping on his/her own and helped to tidy up the entire workshop.		

(5)

Simulation 4A: [25]

Simulation 4B: PICAXE

4.4.8 **Purpose:**

To test knowledge of flow diagrams and PICAXE.

Using PICAXE, draw a flowchart of a control system that counts cars entering and leaving a car park using two digital sensors.

FACET SHEET FOR SIMULATION 4B: PICAXE FLOWCHART

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Start/Stop element	Element placed correctly (1)				1	
Decision element	One decision element placed correctly (1)	Two decision elements placed correctly (2)	Three decision elements placed correctly (3)	Four decision elements placed correctly (4)	4	
Process element	One process element placed correctly (1)	Two process elements placed correctly (2)	Three process elements placed correctly (3)		3	
Data elements	One data element placed correctly (1)	Two data elements placed correctly (2)	Three data elements placed correctly (3)		3	
Flow lines	25% of flow lines placed correctly (2)	50% of flow lines placed correctly (4)	75% of flow lines placed correctly (6)	All flow lines placed correctly (8)	8	
Labelling of elements	3 labels placed correctly (1)	6 labels placed correctly (3)	9 labels placed correctly (5)	All labels placed correctly (6)	6	
				FACET 4B	25	

- Simulation 4A: (25)
 - Simulation 4B: (25)
- Total: Simulation 4: [50]

Please turn over

5. **SECTION B: DESIGN AND MAKE**

Design and Make Project		
Time: January to August 202	1	
Learner Name:		C. Branna
School:		
Class:		
Title/Type of Project:		

INSTRUCTIONS

- This section is COMPULSORY for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
 - Seven components 0
 - A variety of components (both active and passive) 0
 - PCB making in some form 0
 - Soldering 0
 - An enclosure with a switch and protection 0
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST

The learner MUST fill in this checklist for the teacher BEFORE marking of that section takes place!

NO.	DESCRIPTION	TIC	(図)
		NO	YES
Design	and Make: Part 1		
1.	Circuit diagram drawn		
2.	Circuit description filled in		
3.	Component list completed		
4.	Tools list for circuitry populated		
5.	Measuring instrument list filled in		
6.	Evidence of prototyping printed and pasted into the file		
7.	Learner's own Veroboard/PCB planning/design printed and included in file		
Design	and Make: Part 2		
1.	Enclosure design completed and included in the file		
2.	Unique name written down and on the enclosure		
3.	Logo designed and on the enclosure		
Miscell	aneous		
1.	Enclosure included in the project		
2.	Enclosure prepared and drilled according to the design		
3.	Enclosure finished off and completed with name and logo		
4.	PCB securely mounted in the enclosure using acceptable techniques		
5.	Circuit inside the enclosure accessible		
6.	Internal wiring neat and ready for inspection		
7.	File and project completed and ready for moderation at the workshop/room		

5.1 **Design and Make: Part 1**

5.1.1 **Circuit diagram**

Draw a circuit diagram of your project and add it after this page.

5.1.2 **Project: Description of operation**

Use the space below to provide an overview of how the project operates. Do research and use your own words.

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Component list 5.1.3

List the components you will need for the circuit diagram.

LABEL	DESCRIPTION AND VALUE	QUANTITY

5.1.4 **Tools/Instrument List**

List the tools needed to complete the project.

DESCRIPTION	PURPOSE

5.1.5 **Evidence of prototyping**

Take photographs of the working prototype on the breadboard using a digital camera or cellphone and insert it here. Write your name on the photograph.

5.1.6 PCB design

Design a printed circuit board layout for the circuit you are going to build.

Print it out and insert it here.

5.2 Assessment of the Design and Make Phase: Part 1

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *
Circu	it Diagram (10)		
1.	The circuit diagram was drawn using EGD equipment.	1	
2.	The circuit diagram was drawn using CAD/any electronic design software.	1	
3.	The circuit diagram was drawn using correct symbols.	2	
4.	The circuit diagram has all labels – R1, C1, Tr1, etc.	2	
5.	The circuit diagram has all component values -100Ω , 220 µF, etc.	2	
6.	The circuit diagram has a name/title.	1	
7.	The circuit diagram has a frame and title block. (EGD approach).	1	
Com	ponent List (3)		
8.	Labels correlate with circuit diagram.	1	
9.	Description and values correlate with circuit diagram.	1	
10.	Quantities are correct.	1	
Desc	ription of Operation (10)		
11.	Basic function of the circuit is described correctly.	2	
12.	All subcircuits in the circuit diagram and component list are included in the description.	3	
13.	Purposes of subcircuits in the circuit diagram are described correctly.	3	
14.	Learner used own interpretation and did not copy from another source verbatim.	1	
15.	Sources are acknowledged.	1	
	/Instrument List (2)		
16.	The tools/instrument list has been completed.	1	
17.	The tools/instruments listed all have a purpose for being used.	1	
Evide	ence of Prototyping on Breadboard (10)	1	
18.	Unique, original photos of the prototyping are included.	1	
19.	Unique, original photos include the learner name.	2	
20.	Photos are clear and in focus: All components are clearly identifiable.	2	
21.	Prototype is operational. No photo, no mark.	5	
	Design (15) (If a kit is used in this section = 0)	1	
22.	Printed Circuit Board design is included in the PAT file.	1	
23.	PCB Design is made using a CAD approach.	5	
24.	Component overlay showing placement is included.	1	
25.	Components are labelled the same as in the circuit diagram.	1	
26.	The design is original and does not match any other learner's design.	2	
27.	Board layout (tracks/current flow) is functional and matches the original circuit diagram.	5	

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *		
Circu	Sircuit Board Manufacturing (70)				
28.	Circuit board is etched neatly according to the PCB design.	10*			
29.	The learner's name is etched onto the circuit design.	2			
30.	Holes are drilled neatly and are aligned in the middle of the pads on the PCB.	2			
31.	Mounting holes of the PCB are drilled symmetrically.	2			
32.	All burrs are removed.	2			
33.	The PCB is cut neatly/squarely and edges are filed neatly.	2			
34.	Axial and radial components are placed neatly and flush with the board.	2			
35.	Component orientation are aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2			
36.	Soldered components – leads are cut off, flush and neat on the solder side.	3			
37.	More than 60% of the solder joints are shiny (not dry joints).	5			
38.	Wire insulation is stripped to the correct length (no extra copper showing).	3			
39.	Wiring is long enough to allow for dismantling and inspection.	2			
40.	Wiring is wrapped neatly.	2			
41.	A power switch is included and fitted to the enclosure.	2			
42.	A fuse/Protection is included and fitted correctly where applicable.	2			
43.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2			
44.	Batteries are mounted using a battery housing/mounting bracket and battery clip (NO double-sided tape).	2			
45.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. (Switch is on – must go out when fuse is blown.)	3			
46.	The project is fully operational and commissioned/installed in the enclosure.	20			

TOTAL	
(PART 1 = 120 marks)	

In projects where facets are not applicable, the projects should be marked and the totals adjusted accordingly. NOTE:

5.3 Design and Make: Part 2

5.3.1 Enclosure design

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.
- 5.3.2 Manufacture the enclosure neatly according to your design.
 You may use pre-cut panels from metal, wood and/or Perspex/Plexiglass. You must, however, construct/assemble these parts.
 Injection moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.
- 5.3.3 Choose a name for your device. Write down the name of the device below.
- 5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page.

[30]

5.4 Assessment of the Design-and-Make-Phase: Part 2

	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = *		
Enclo	Enclosure Design (10)				
1.	Enclosure design is included in first-angle orthographic projection.	2			
2.	Drawn design includes a title box and page border.	1			
3.	Isometric drawing included additionally.	2			
4.	Dimensions are included.	2			
5.	The name of the device is written in the PAT document.	1			
6.	The logo design and specification plate design is in the PAT document.	2			
	Subtotal (10 mark	s max.)			
Enclo	sure Manufacturing (20)				
7.	Enclosure matches the design.	1			
	 Dimensions and placement correlate. 	I			
8.	Name of the device is attached on the enclosure.	1			
9.	The logo design is attached on the enclosure.	2			
10.	The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen	2			
	printed/sublimation printed).				
11.	The enclosure is manufactured from scratch/pre-cut parts. Does NOT include: cardboard, paper, margarine container Does include: sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes	5			
12.	Holes/Cut-outs in the enclosure are made with the appropriate tools.	3			
13.	Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project.	2			
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2			
15.	The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.)	2			
	Subtotal (20 mark	s max.)			

TOTAL	
(PART 2 = 30 marks)	

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6. **PROJECTS**

Practical Project 6.1: Traffic light

This project operates red, amber and green LEDs in the correct sequence for a single traffic light. The time taken for the complete red-red and amber-green-amber sequence can be varied from about 7 s to about 2½ minutes by adjusting the 1M pre-set. Some amber LEDs emit light that is almost red so you may prefer to use a yellow LED.

The 555 astable circuit provides clock pulses for the 4017 counter which has ten outputs (Q0 to Q9). Each output becomes high in turn as the clock pulses are received. Appropriate outputs are combined with diodes to supply the amber and green LEDs. The red LED is connected to the ÷10 output which is high for the first 5 counts (Q0 to Q4 high), this saves using 5 diodes for red and simplifies the circuit.



COMPONENT LIST			
RESISTORS	CAPACITORS	DIODES	
R1 100 k Ω	C1 1 µF	LED GREEN	
R2 220 Ω	C2 1 µF	LED YELLOW	
R3 220 Ω	C3 10 µF	LED RED	
R4 220 Ω		D1 1N4007 X 6	
R5 22 kΩ		IC CD 4017	
R6 470 kΩ (adjustable resistor)		IC NE555	

Practical Project 6.2: Two-digit object/product counter

In this circuit, a comparator (IC LM358), an IR transmitter and a receiver pair were used to detect an object. A 555 timer IC was used to generate a pulse for triggering the 7-segment decoder (CD4033) and two common cathode 7-segment display units are connected with a 7-segment decoder IC. A 555 timer IC is configured in mono-stable mode for generating pulse. An LM7805 voltage regulator is used to provide a constant 5-volt power supply for the circuit. A 9-volt battery is used to power the whole circuit.



TWO-DIGIT OBJECT/PRODUCT COUNTER CIRCUIT

COMPONENT LIST			
RESISTORS	CAPACITORS	DIODES	
R1 10 kΩ	C6 220 µF	D1 LED RED	
R2 10 kΩ	IC CD 4017	D2 LED	
R3 150 Ω	IC CD4033	D3 IR T _X	
R4 150 Ω	IC NE555	D4 IR R _x	
R5 150 Ω	IC LM358	D1 1N4007 X 6	
R6 10 kΩ	Voltage regulator 7805		
R7 100 kΩ	7-segment display		
RV_1 10 k Ω (adjustable resistor)	7-segment display		

Operation

In this circuit we detect objects by using an IR sensor and a comparator. Then we apply the output of the comparator to the mono-stable multi-vibrator. This mono-stable multi-vibrator generates a pulse of a fixed time period which can be set by using a given formula.

After getting a pulse from the 555 timer, this pulse is applied to the clock pin of the 7-segment decoder (U4) and then carries out the signal (pin 5) to clock pin of the other 7-segment decoder (U3). After getting a pulse from the 555 timer, the 7-segment counter changes the number value of the segment display and when the number counting reaches 10 in the U4 decoder, it then sends a carry-out signal or pulse to the second 7-segment decoder (U3). Then the second display changes its number value. This process repeats itself. This object counter circuit can count from 00 to 99.

NOTE: All circuits MUST include an on/off switch with an ON indicator and fuse protection.

7. CONCLUSION

On completion of the practical assessment task learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.