basic education

Department:
Basic Education
REPUBLIC OF SOUTH AFRICA

ELECTRICAL TECHNOLOGY (DIGITAL ELECTRONICS)

GUIDELINES FOR PRACTICAL ASSESSMENT TASKS (PAT)

GRADE 12

2022

These guidelines consist of 42 pages.

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1. INTRODUCTION

The 18 Curriculum and Assessment Policy Statements subjects which contain a practical component all include a practical assessment task (PAT). These subjects are:

- AGRICULTURE: Agricultural Management Practices, Agricultural Technology
- ARTS: Dance Studies, Design, Dramatic Arts, Music, Visual Arts
- SCIENCES: Computer Applications Technology, Information Technology, Technical Sciences; Technical Mathematics
- SERVICES: Consumer Studies, Hospitality Studies, Tourism
- TECHNOLOGY: Civil Technology, Electrical Technology, Mechanical Technology and Engineering Graphics and Design

A practical assessment task (PAT) mark is a compulsory component of the final promotion mark for all candidates offering subjects that have a practical component and counts 25% (100 marks) of the end-of-the-year examination mark. The PAT is implemented across the first three terms of the school year. This is broken down into different phases or a series of smaller activities that make up the PAT. The PAT allows for learners to be assessed on a regular basis during the school year and it also allows for the assessment of skills that cannot be assessed in a written format, e.g. test or examination. It is therefore important that schools ensure that all learners complete the practical assessment tasks within the stipulated period to ensure that learners are resulted at the end of the school year. The planning and execution of the PAT differs from subject to subject.

Practical assessment tasks are designed to develop and demonstrate a learner's ability to integrate a variety of skills in order to solve a problem. The PAT also makes use of a technological process to inform the learner what steps needs to be followed to derive a solution for the problem.

The PAT consists of four simulations and a practical project. The teacher may choose any ONE of the practical projects and any TWO simulations available for DIGITAL ELECTRONICS.

The teacher must apply assessment on an ongoing basis at the same time that the learner is developing the required skills. TWO simulations should be completed by the learners, in addition to the manufacturing of a practical project.

The PAT incorporates all the skills the learner has developed throughout the year. The PAT ensures that all the different skills will be acquired by learners on completion of practical work, as well as the correct use of tools and instruments.

Requirements for presentation

A learner must present the following:

- PAT file with all the evidence of simulations, design and prototyping. A copy of the PAT 2022 cover page. The relevant simulations and assessment sheets should be copied and handed to each learner to include in the file.
- Practical project with:
  - Enclosure:
    - The file must include a design.
    - The enclosure and the design must match.
    - No cardboard boxes are allowed.
    - Plastic wooden and metal enclosures are acceptable.
    - Enclosures that are manufactured and/or assembled by the learners are preferred.
    - The enclosure should be accessible for scrutiny inside.
    - Lids that are secured are preferred.

- Circuit board:
  - The file should include the PCB design.
  - The PCB must be mounted inside the enclosure in such a manner that it can be removed for scrutiny. Alternatively, inspection can be made from the bottom in cases where translucent (see-through) enclosures are used.
  - Switches, potentiometers, connectors and other items must be mounted.
  - Wiring must be neat and bound/wrapped.
  - Wiring must be long enough to allow for the PCB to be removed and inspected with ease.
- Logo and name:
  - The file should contain the logo and name design and specification plate.
  - Logo, specification plate and name must be prominent on the enclosure.
  - The logo/specification plate must be affixed in a permanent manner – painted, glued or stuck on with vinyl

The PAT will have a financial impact on the school's budget and school management teams are required to make provision to accommodate this particular expense.

PAT components and other items must be acquired timeously, for use by the learners, before the end of the first term at the start of the academic year.

It is the responsibility of the HOD to ensure that the teacher is progressing with the PAT from the start of the school year.

Provincial departments are responsible for setting up moderation timetables and consequently PATs should be completed in time for moderation.

2. TEACHER GUIDELINES

2.1 How to administer PATs

Teachers must ensure that learners complete the simulations required for each term. The project should be started in January in order to ensure its completion by August. In instances where formal assessments take place, the teacher has to assume the responsibility thereof.

The PAT should be completed during the FIRST THREE TERMS and must be ready at the start of PAT moderation. Teachers must make copies of the relevant simulations and hand them to learners at the beginning of each term.

The PAT must not be allowed to leave the workshop and must be kept in a safe place at all times when learners are not working on them.

The weightings of the PAT must be adhered to and teachers are not allowed to change weightings for the different sections.

2.2 How to mark/assess the PATs

The PAT for Grade 12 will be set and assessed internally, but moderated externally. All formal assessment will be done by the teacher.

The teacher is required to produce a **working model and model answer file** that sets the baseline for assessment at a Highly Competent Level for every project choice exercised by the learners. This file must include all the simulations with answers the teacher has done him/herself. The teacher will use the model answers and project to assess the simulations and projects of the learners.

Once a facet sheet has been completed by the teacher, assessment will be deemed to be complete. **No re-assessment will be done once the facet sheets have been completed** and captured by the teacher. Learners must ensure that the work is done to the required standard before the teacher finally assesses the PAT during each stage of completion.

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2.3 PAT Programme of Assessment (PAT PoA)

The programme of assessment (PoA) of the PAT is as follows:

TIME FRAME	ACTIVITY	RESPONSIBILITY
	Preparation for PAT 2022	Teacher – Builds the models and works out the model answers for the simulations for 2022. Identifies shortages in tools, equipment and consumable items for simulations that must be procured in 2022 SMT – Receives procurement requests from teachers and processes payments for the acquisition of required items
January–March 2022	Simulation 1	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
January 2022	PAT project – procurement	Teacher – Obtains quotations for PAT projects Principal – Approves PAT procurement for PAT projects Teacher – Ensures that PAT projects are ordered and delivered HOD – Checks in on teacher to see if the process is adhered to
February 2022	PAT project – learners commence with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Commence with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
April–June 2022	Simulation 2	Teacher – Copies and hands out simulations Learners – Complete simulations Teacher – Assesses simulations HOD – Checks if tasks have been completed and marked by the teacher before the holiday
April–June 2022	Moderation of Simulation 1	District subject facilitator/subject specialist will visit the school and moderate Simulation 1 10% of learners' work is moderated
April–June 2022	PAT project – learners continue with project	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Includes practical sessions for learners to complete the PAT project every week Learners – Continue with completion of the PAT project HOD – Checks in on teacher to ensure that practical workshop sessions take place on a weekly basis
July holidays 2022	PAT intervention	Learners that are behind on the PAT are required to complete the project during this holiday.
July–August 2022	Moderation of Simulation 2	District subject facilitator/subject specialist will visit the school and moderate Simulations 2 – different learners from the previous term 10% of learners' work is moderated
July–August 2022	PAT project – completion	Teacher – Ensures that there is secure storage for PAT projects Teacher – Hands out and takes in PAT projects Teacher – Completes the PAT project with learners and compiles the PAT file Learners – Complete the PAT project and file HOD – Checks to see that 100% of the PAT files and projects are completed and assessed
September–October 2022	PAT moderation	PAT projects are moderated by subject facilitators/subject specialists from the province and learners are available to demonstrate skills 10% of learners are moderated randomly

2.4 Moderation of PATs

Provincial moderation of each term's simulations will start as early as the following term. Simulations 1 should be moderated as soon as the second term starts. Similarly, Simulation 2 will be moderated in July. The project will, however, only be moderated on completion.

During moderation of the PAT the learner's file and project must be presented to the moderator.

The moderation process is as follows:

- During moderation, learners are randomly selected to demonstrate the different simulations. Both simulations will be moderated.
- **The teacher is required to build a model of each project chosen for the school.**
- **This model must be on display during moderation.**
- **The teacher's model forms the standard of the moderation at Level 4 (Highly Competent).**
- **Level 5 assessments must exceed the model of the teacher in skill and finishing.**
- Learners who are moderated will have access to their files during moderation and may refer to the simulations they completed earlier in the year.
- Learners may NOT ask assistance from other learners during moderation.
- All projects and files must be on display for the moderator.
- **If a learner is unable to repeat the simulation or cannot produce a working circuit during moderation, marks will be deducted and circuits assessed as not being operational.**
- The moderator will randomly select no fewer than **two projects** (not simulations) and the learners involved will have to explain how the project was manufactured/built.
- Where required, the moderator should be able to call on the learner to explain the function and principles of operation, and request the learner to exhibit the skills acquired through the simulations for moderation purposes.
- On completion the moderator will, if needed, adjust the marks of the group upwards or downwards, depending on the outcome of moderation.
- Normal examination protocols for appeals will be adhered to, if a dispute arises from adjustments made.

2.5 Absence/Non-submission of Tasks

The absence of a PAT mark in Electrical Technology without a valid reason: The learner will be given three weeks before the commencement of the final end-of-year examination to submit outstanding task. Should the learner fail to fulfil the outstanding PAT requirement, such a learner will be awarded a zero (0) for that PAT component.

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2.6 Simulations

Simulations are circuits, experiments and tests which the learner will have to build, test and measure and practically do as part of the development of practical skills. These skills have to be illustrated to the external moderator that visits the school at intervals during the school year.

Teachers who use simulation programs on a computer may use them for the learners to practice on. However, it is required that the circuit be built using real components and that measurements be made with actual instruments for the purposes of assessment and moderation.

The correct procedure for completing simulations is outlined below for teachers and school management teams who are responsible for the implementation of the PAT in Electrical Technology.

STEP 1: The teacher will choose simulations from the provided examples.
STEP 2: Compile a list of the components needed for every simulation. Add extra components as these items are very small and you will need extras, as these items are lost/damaged very easily when learners work with them.
STEP 3: Contact three different electronics component suppliers for comparative quotations.
STEP 4: Submit the quotations to the SMT for approval and procurement of the items.
STEP 5: Place the components in storage. Collate items for each simulation, thus making it easier to distribute and use during practical sessions. Ensure that different values of components do not mix, as this would lead to components being used incorrectly and this could damage the component and in extreme cases, the equipment used.
STEP 6: Copy the relevant simulations and hand them out to learners at the start of the term.

Teachers are allowed to adjust circuits and component values to suit their environment/ resource availability.

Teachers are required to develop a set of model answers in the teacher's file.

Moderators will use the teacher's model answers and artefacts when moderating.

2.7 Projects

The projects are construction projects teachers can choose for their learners. These projects are based on circuits provided by schools and subject advisors. The projects are based on working prototypes and require careful construction in order for it to operate correctly.

Projects vary in cost and teachers must ensure that the projects chosen fall within the scope of the school's budget.

Once the teacher has decided on a circuit, he/she must construct the prototype. Thereafter, copies of the provided circuit can be made and distributed to learners. They MUST redraw these circuits in their portfolios correctly.

The description of the operation of the circuits is NOT complete. Learners are required to interrogate the function of the components in the provided circuit. They should elaborate on the purpose of components in the circuit. It is recommended that learners investigate similar circuits available on the internet and in the school library or workshop reference books.

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2.8 Working mark sheet

(A working Excel file is provided with this PAT)

PAT mark sheet		**Term 1**	**Term 2**	**Project**				
No.	**Name of Learner**	**Simulation 1** **50**	**Simulation 2** **50**	**Design and Make Part 1** **120**	**Design and Make Part 2** **30**	**Total = Term 1 + Term 2 + Project** **250**	**Mark out of 100**	**Moderated Mark**
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								
	Total							
	Average							

Teacher Name: _____ Principal Name: _____ Moderator Name: _____

Signature: _____ Signature: _____ Signature: _____

Date: _____ Date:_____ Date:_____

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3. LEARNER GUIDELINES

PAT 2022 cover page (Place this page at the front of the PAT.)

Department of Basic Education
Grade 12
CAPS for Technical High Schools
Practical Assessment Task – Electrical Technology

Time allowed: Terms 1–3 (2022)

Learner Name: _____

Class: _____

School: _____

Specialisation: DIGITAL ELECTRONICS

Complete TWO simulations.

Project (Write the name of the project): _____

Evidence of moderation:

NOTE:
When the learner evidence (LE) selected has been moderated at school level, the table will contain evidence of moderation. Provincial moderators will sign the provincial moderation and only sign if re-moderation is needed.

Moderation	Signature	Date	Signature	Date
School-based				
District moderation				
Provincial moderation			Re-moderation	

Mark allocation

PAT Component	Maximum Mark	Learner Mark	Moderated Mark
Simulation 1	50		
Simulation 2	50		
Design and Make Project – Circuit	120		
Design and Make Project – Enclosure	30		
Total	**250**		

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3.1 Instructions to learners

- The practical assessment task counts 25% of your final promotion mark.
- All work produced by you must be your own effort. Group work is NOT allowed.
- The practical assessment task must be completed over three terms.
- The PAT file must contain TWO simulations and a practical project.
- Calculations should be clear and include units. Calculations should be rounded off to TWO decimals. SI units should be used.
- Circuit diagrams can be hand-drawn or drawn on CAD. NO photocopies or scanned files are allowed.
- Photos are allowed and may be in colour or greyscale. Scanned photos and photocopies are allowed.
- Learners with identical photos will be penalised and receive zero for that section.
- This document must be placed inside your PAT file together with the other evidence.

3.2 Declaration of Authenticity (COMPULSORY)

Declaration:

I _____ (Name) herewith declare that the work represented in this File/evidence is entirely my own effort. I understand that if proven otherwise, my final results may be withheld.

_____
Signature of learner

_____
Date

4. SIMULATIONS

4.1 Simulation 1A: Monostable multivibrators using a 555 IC

Name of learner: _____	
Class: _____ **Date Completed:** _____	**Mark** _____ / 50
Date Assessed: _____	Assessor Signature: _____
Date Moderated: _____	Moderator Signature: _____

4.1.1 **Purpose:**

- To study a monostable multivibrator using a 555 IC.
- To build a monostable multivibrator with the 555 IC.
- To compare the theory learned in class with the actual circuit.

4.1.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Breadboard Voltmeter (multimeter) DC power supply, 5 V Side cutters Long-nose pliers Wire stripper	1 x 555 IC 2 x 10 kΩ resistors 1 x 1 kΩ resistor 2 x 470 Ω resistors 1 x 220 µF electrolytic capacitor, 16 V 1 x LED 1 x push button/tactile switch Connecting wires

4.1.3 **Procedure:**

Build the circuit diagram in FIGURE 4.1.3 on your breadboard.
After the teacher has checked the circuit, switch the power ON.
Connect a multimeter to measure the voltage on pin 2.
Connect a multimeter to measure the voltage across C_1.

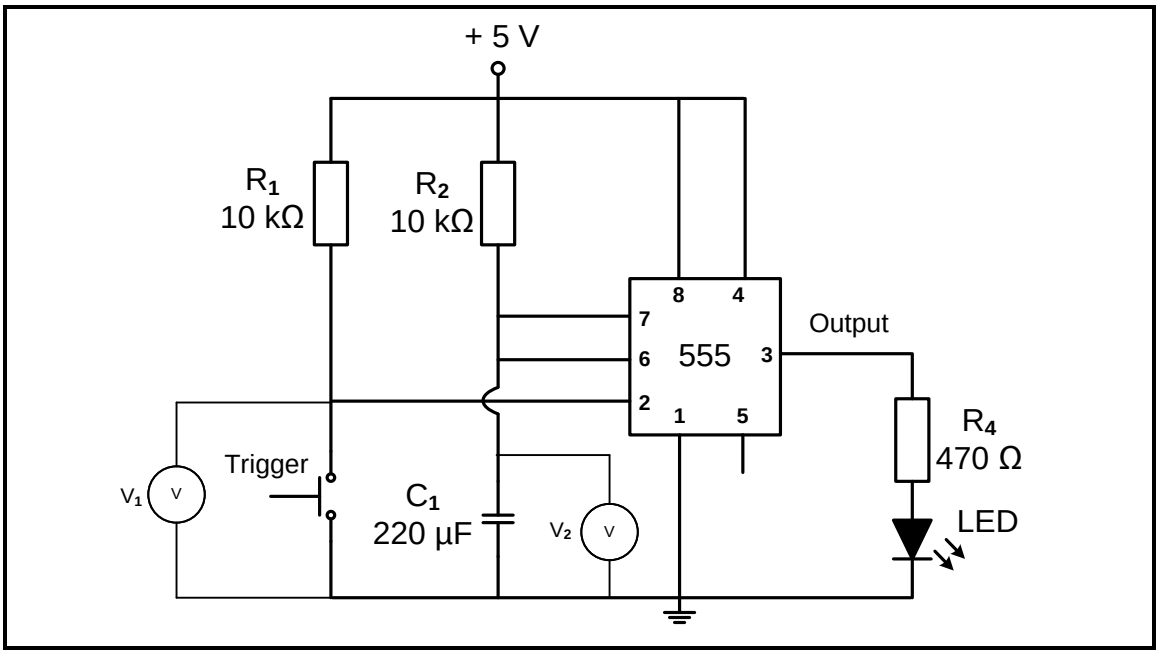

FIGURE 4.1.3: MONOSTABLE MULTIVIBRATOR

(a) Write down the voltage measured across pin 2.

Voltage on pin 2 V_1 = _____ (2)

(b) State the function of R_1 with reference to pin 2 and the output. (2)

_____

_____

(c) Press switch S_1 and observe what happens to the voltage measurement across the capacitor. Write down the voltage measured across C_1 just before the LED switches OFF (maximum charged voltage).

Voltage across C_1. V_2 = _____ (2)

(d) Compare the voltage across C_1 to the supply voltage. (2)

_____

_____

(e) Press switch S_1 twice within a short time frame to simulate switch bounce. Write down your observation. (4)

_____

_____

_____

_____

_____

(f) Replace capacitor C_1 with a 100 µF capacitor. Switch ON the circuit, press switch S_1 and observe. Write down your observation and give a reason why this happens. (4)

_____

_____

_____

Simulation 1A: [16]

FACET SHEET OF SIMULATION 1A: MONOSTABLE MULTIVIBRATOR

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – multimeter (1)	Collect hand tools (1)	4	
Hand tools	Use hand tools (1)				1	
Preparation for insertion of components into breadboard	Check the pin-out of the 555 IC on the relevant data sheet (1)	Set supply voltage at +5 V (1)			2	
Correct connection on breadboard – nodes and polarity	Correct connection of 555 IC to the supply (2)	Polarity and connection of switches – correct (1)	Polarity LED – correct (1)		4	
Circuit is working correctly	S1 is pressed – LED 1 (red) ON (1)	LED stays on in relation to the RC time constant (1)			2	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in places after work (1)			2	
Safety	Observing safety before being reminded (2)	Observing safety after being reminded (1)			2	
				Facet sheet of Simulation 1A:	**[17]**	

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Simulation 1B: Astable multivibrator

4.1.4 **Purpose:**

- To build an electronic piano (astable multivibrator) using the 555 IC in FIGURE 4.1.6 on a breadboard and display the output waveforms on an oscilloscope.

4.1.5 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Analogue/Digital oscilloscope Function generator Variable DC power supply Side cutters Wire stripper	1 x 555 timer IC 1 x 100 nF capacitor 1 x 10 µF (electrolytic capacitor, 25 V) 5 x 1 kΩ resistor 1 x 10 kΩ potentiometer 1 x 8 Ω speaker/buzzer 5 x push buttons Connecting wires

4.1.6 **Procedure:**

(a) Build the circuit in FIGURE 4.1.6 on the breadboard.
Connect channel 1 of the oscilloscope to pin 3 of the 555 IC.
Switch ON the circuit, press the push buttons (one at a time) and observe.
Answer the questions that follow.

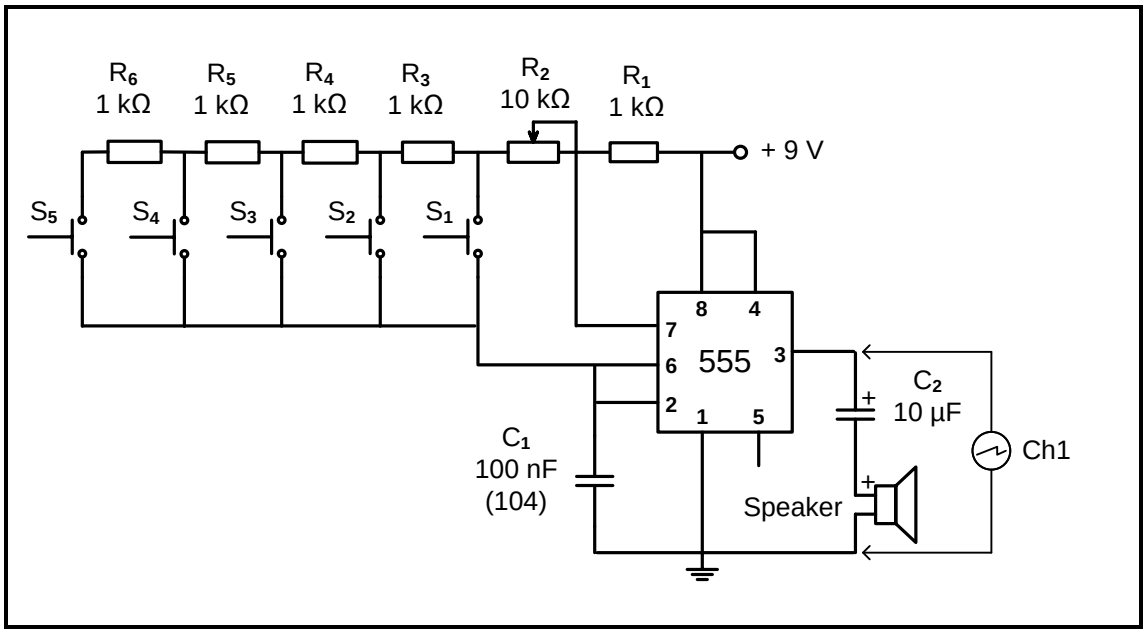
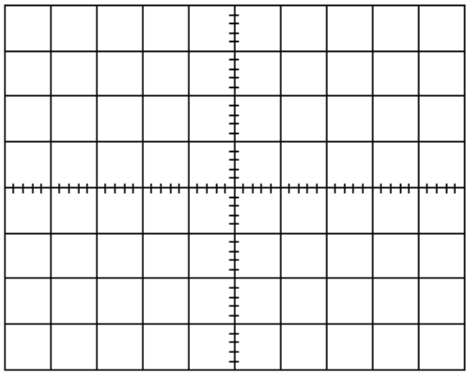


FIGURE 4.1.6: ASTABLE MULTIVIBRATOR

If there is noise, pin 5 can be connected to ground via a capacitor of 0,01 µF.

(b) Press push button S_1 and draw the output wave observed on the oscilloscope grid provided. Set the oscilloscope to display at least FOUR complete cycles.



V/Div:_____ (Ch 1)

T/Div: _____

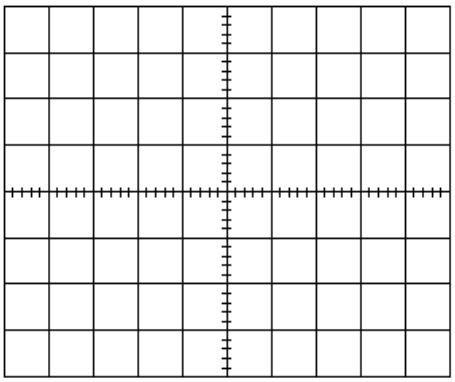
NOTE: 1 mark for the correctly drawn waveform. 1 mark for the oscilloscope settings.

(2)

(c) Make use of the oscilloscope settings and determine the frequency of the signal.

Frequency when S_1 is pressed _____ (2)

(d) Press push button S_5 and draw the output wave observed on the oscilloscope grid provided. Do NOT adjust the time per division setting.



V/Div:_____ (Ch 1)

T/Div: _____

NOTE: 1 mark for the correctly drawn waveform. 1 mark for the oscilloscope settings.

(2)

(e) Make use of the oscilloscope settings and determine the frequency of the signal.

Frequency when S_5 is pressed _____ (2)

(f) Press each of the push buttons and observe.
Explain why there is a difference in the output for each push button. (3)

Simulation 1B: [11]

RUBRIC FOR SIMULATION 1B

0	1	2	LEARNER MARK
Learner was not able to connect the circuit correctly	Learner was able to connect a part of the circuit correctly without assistance	Learner was able to connect the whole circuit correctly without assistance	
The learner was not able to display the output wave on the oscilloscope	The learner was able to set the oscilloscope and managed to get the output wave after the assistance from the teacher	The learner was able to set the oscilloscope and managed to get the output wave without the assistance of the teacher	
Learner did not do any housekeeping duties	Learner did housekeeping after being reminded	Learner did housekeeping without being reminded	

(6)

Simulation 1A: (16)
Facet sheet of Simulation 1A: (17)
Simulation 1B: (11)
Rubric of Simulation 1B: (6)
TOTAL SIMULATION 1: **[50]**

4.2 Simulation 2A: Switching circuits using a 555 IC and a 741 op-amp

Name of learner: _____	**Mark** _____ / 50
Class: _____ **Date completed:** _____	
Date Assessed: _____	Assessor Signature: _____
Date Moderated: _____	Moderator Signature: _____

4.2.1 Purpose:

- To build the monostable multivibrator in FIGURE 4.2.3 using a 555 IC.
- To compare the theory learned in class with the actual circuit.

4.2.2 Required Resources:

TOOLS/INSTRUMENTS	MATERIALS
Experiment board Voltmeter (multimeter) DC power supply, 5 V Side cutters Long-nose pliers Wire stripper	1 x 555 IC 2 x 10 kΩ resistors 1 x 1 kΩ resistors 2 x 470 Ω resistors 1 x 220 µF electrolytic capacitor, 16 V 1 x 220 µF electrolytic capacitor, 16 V 1 x LED 1 x push button/tactile switch Connecting wires

4.2.3 Procedure:

Build the circuit diagram in FIGURE 4.2.3 on your experiment board.
After the teacher has checked the circuit, switch the power ON.
Connect a multimeter to measure the voltage on pin 2.
Connect a multimeter to measure the voltage across C_1.

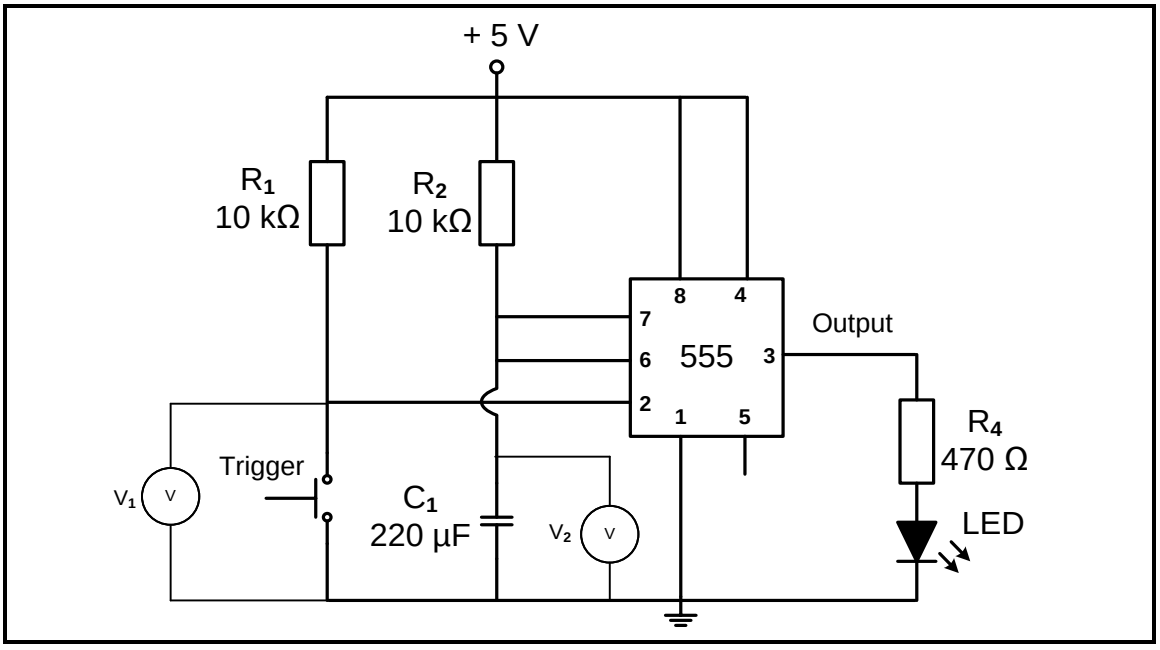


FIGURE 4.2.3: 555 MONOSTABLE MULTIVIBRATOR

(a) Write down the voltage measured across pin 2.

Voltage across pin 2 V_1 = _____ (1)

(b) State the function of R_1 with reference to pin 2 and the output. (2)

_____

_____

(c) Press the trigger input and observe what happens to the voltage measurement across the capacitor. Write down the voltage measured across C_1 just before the LED switches OFF (maximum charged voltage).

Voltage across C_1. V_2 = _____ (1)

(d) Compare the voltage across C_1 to the supply voltage. (2)

_____

_____

(e) Press the trigger input twice within a short time frame to simulate switch bounce. Write down your observation. (3)

_____

_____

_____

_____

(f) Replace capacitor C_1 with a 100 µF capacitor. Switch ON the circuit, press the trigger input and observe. Write down your observation and give a reason why this happens. (4)

_____

_____

_____

(g)

Learner was able to construct a minimum part of the circuit correctly without assistance.	Learner was able to construct a part of the circuit correctly without assistance.	Learner was able to construct the circuit correctly without assistance.
1	**3**	**4**

(4)

Simulation 2A: (17)

Simulation 2B: Inverting op-amp using 741 IC

4.2.4 **Purpose:**

- To build the inverting amplifier circuit in FIGURE 4.2.6(a) using a 741 op-amp and display the output waveforms on an oscilloscope.
- To investigate the effect of ratio RF to RIN on the gain and the output of the amplifier.

4.2.5 **Required Resources:**

TOOLS/INSTRUMENTS	MATERIALS
Function generator Dual-trace oscilloscope +9 V 0 V–9 V DC power supply Side cutters Wire stripper Calculator	1 x LM741 op-amp 1 x 100 kΩ resistor 1 x 68 kΩ resistor 1 x 47 kΩ resistor 1 x 22 kΩ resistor 1 x 10 kΩ resistor Connecting wires

4.2.6 **Procedure:**

Set the dual voltage power supply to +9 V/-9 V.
Set the function generator to deliver a 0,5 V peak 1 kHz sine wave.
Build the circuit in FIGURE 4.2.6(a) on your experiment board and connect it to the supply and input.
Connect channel 1 of the oscilloscope across the input to display at least TWO complete cycles.
Connect channel 2 of the oscilloscope across the output to display at least TWO complete cycles.

(a) Build the circuit in FIGURE 4.2.6(a) on the experiment board.

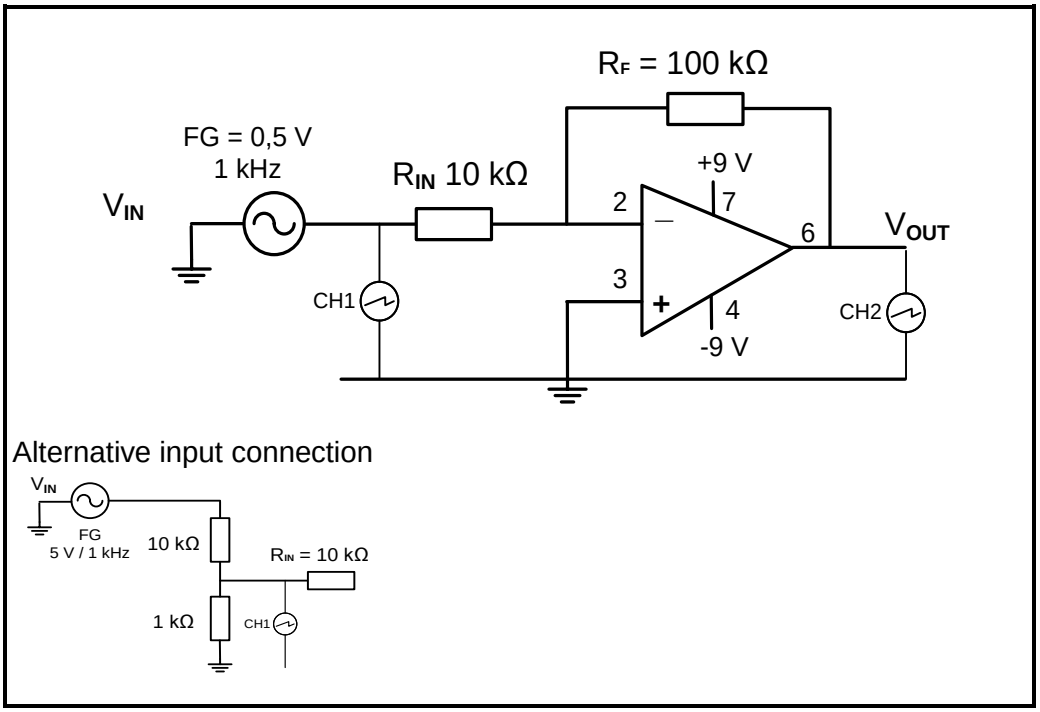
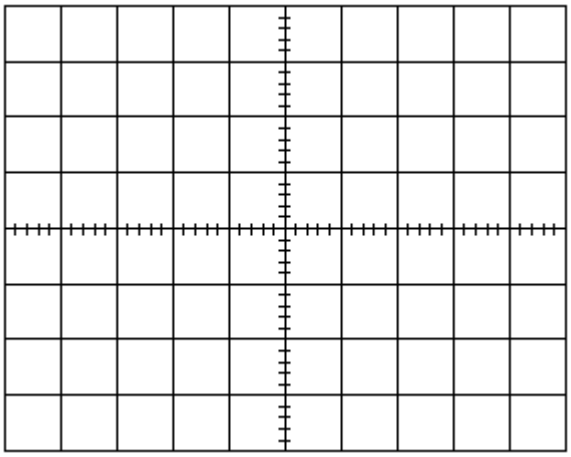


FIGURE 4.2.6 (a): 741 INVERTING OP-AMP

(b) Draw the input and output waveforms on the oscilloscope grid provided in OSCILLOGRAM 4.2.6(b) below.



V/Div:_____ (Ch 1)

V/Div:_____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

(5)

OSCILLOGRAM 4.2.6(b)

(c) Use the oscilloscope settings to determine the values of:

V_{IN} = _____ (1)

V_{OUT} = _____ (1)

(d) Calculate the gain of the amplifier using the determined voltage values.

_____

_____

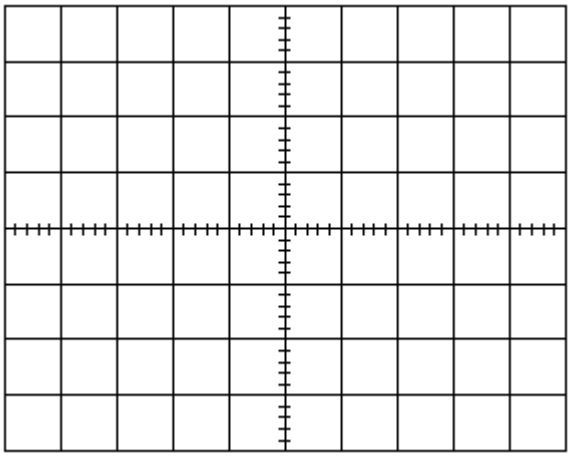
_____ (3)

(e) Replace resistor R_F 100 kΩ with the following resistors and write down the value of the output voltage.

R_F	OUTPUT VOLTAGE
68 kΩ	
47 kΩ	
22 kΩ	
10 kΩ	

TABLE 4.2.6(e) (4)

(f) Draw the input and output waveforms observed on the oscilloscope grid below when R_F is 10 kΩ in OSCILLOGRAM 4.2.6(f).



V/Div:_____ (Ch 1)

V/Div:_____ (Ch 2)

T/Div: _____

NOTE: 1 mark for each correctly drawn waveform. 1 mark for each correct oscilloscope setting.

(5)

OSCILLOGRAM 4.2.6(f)

(g) Calculate the gain of the amplifier when R_F = 10 kΩ.

_____

_____

_____ (3)

(h) Compare the output voltages in TABLE 4.2.6(e) to the input voltage in (c) and write a conclusion.

_____

_____

_____ (3)_

1	3	4
Learner was able to construct a minimum part of the circuit correctly without assistance	Learner was able to construct a part of the circuit correctly without assistance.	Learner was able to construct the circuit correctly without assistance
Learner was able to connect the oscilloscope probes correctly but could not set it up to display the signals.	Learner was able to connect the oscilloscope probes correctly and partially set it up to display the signals.	Learner was able to connect the oscilloscope probes correctly and set it up to display the signals correctly.

(8)

Simulation 2B: (33)

Subtotal simulation 2A: (17)
Subtotal simulation 2B: (33)
TOTAL SIMULATION 2: [50]

4.3 Simulation 3: Connecting a 7-segment display to a 4-bit BCD 7-segment display driver

Name of learner: _____	
Class: _____ **Date Completed:** _____	**Mark** _____ 50
Date Assessed: _____	Assessor Signature: _____
Date Moderated: _____	Moderator Signature: _____

Activity 3A: Connection of a 7-segment display to a 4-bit BCD 7-segment display driver

4.3.1 Purpose:

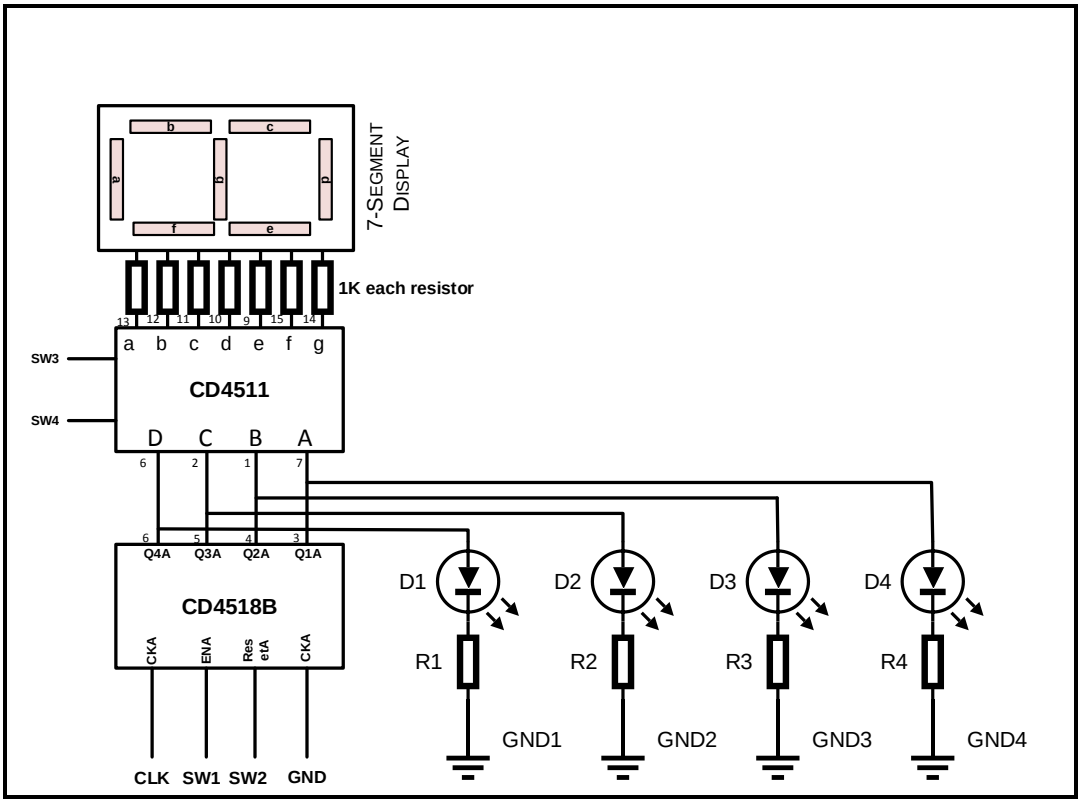
- To connect a 7-segment display to a 4-bit BCD 7-segment display driver.

4.3.2 Required Resources:

TOOLS/INSTRUMENTS	MATERIALS
Analogue/Digital trainer Breadboard Variable DC power supply Side cutters Breadboard wire	4 x LEDs 4 x 390 Ω resistors 7 x 1k resistors CD4511 IC CD4518B IC 5 x SPST switches 7-segment display

4.3.3 Procedure:

Connect the circuit as in the circuit given below:



An alternative circuit can be used

FACET SHEET FOR SIMULATION 3: CONNECT A 7-SEGMENT DISPLAY TO A 4-BIT BCD 7-SEGMENT DRIVER DISPLAY

	FACET 1	FACET 2	FACET 3	FACET 4	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Prepare for the simulation	Identify components correctly (1)	Collect PSU/mini trainer (1)	Collect instruments – oscilloscope (1)	Collect hand tools (1)	4	
Hand tools	Use hand tools correctly (1)				1	
Preparation for insertion of components into breadboard	Check the datasheet on the ICs (1)	Set supply voltage correct at +9 V (1)			2	
Correct connection on breadboard – nodes and polarity	8 nodes for correct connection of CB4518B IC (8)	8 nodes for correct connection of CD4511 IC and the 7-segment display (20/75 = 15)			23	
Housekeeping	Cleaning the working area after the experiment (1)	Placing tools back in places after work (1)			2	
Safety	Observing safety before being reminded (2)	Observing safety after being reminded (1)			3	
				Facet sheet for Simulation 3:	**[35]**	

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Activity 3B

Conduct the following steps and answer the questions in the spaces provided.

STEP	IC CD4185 GIVEN CODE	7-SEGMENT DISPLAY	
(a)	Which number is displayed on the 7-segment display driver if the binary number 0111 is illuminated on the output LEDs of the counter?		(3)
(b)	Which number is displayed on the 7-segment display driver if the binary number 1000 is illuminated on the output LEDs of the counter?		(3)
(c)	Which number is displayed on the 7-segment display driver if the binary number 1001 is illuminated on the output LEDs of the counter?		(3)
(d)	Which number is displayed on the 7-segment display driver if the binary number 0011 is illuminated on the output LEDs of the counter?		(3)
(e)	Which number is displayed on the 7-segment display driver if the binary number 0101 is illuminated on the output LEDs of the counter?		(3)
			[15]

Activity 3A: (35)
Activity 3B: (15)
TOTAL SIMULATION 3: **[50]**

4.4 Simulation 4: JK flip-flop circuit and PICAXE

Name of learner: _____	**Mark** _____ / 50
Class: _____ **Date completed:** _____	
Date Assessed: _____ Assessor Signature: _____	
Date Moderated: _____ Moderator Signature: _____	

Simulation 4A: JK flip-flop circuit

4.4.1 **Purpose:**

- To demonstrate the operation of the JK flip-flop circuit practically.

4.4.2 **Required resources:**

TOOLS/INSTRUMENTS	MATERIALS
Breadboard	SN7476 IC
Voltmeter	Toggle switches x 4
Dual power supply 9 V 0–9 V	1 kΩ resistor x 3
Dual power Supply 5 V 0–5 V	10 kΩ resistor x 1
Side cutters	1 x red and 1 x green LED
Wire stripper	Connecting wires

4.4.3 **Circuit Diagram**

Connect the circuit as in FIGURE 4.3.3 on the breadboard. After you switch on the circuit, press the reset switch. You will be assessed with the rubric that follows.

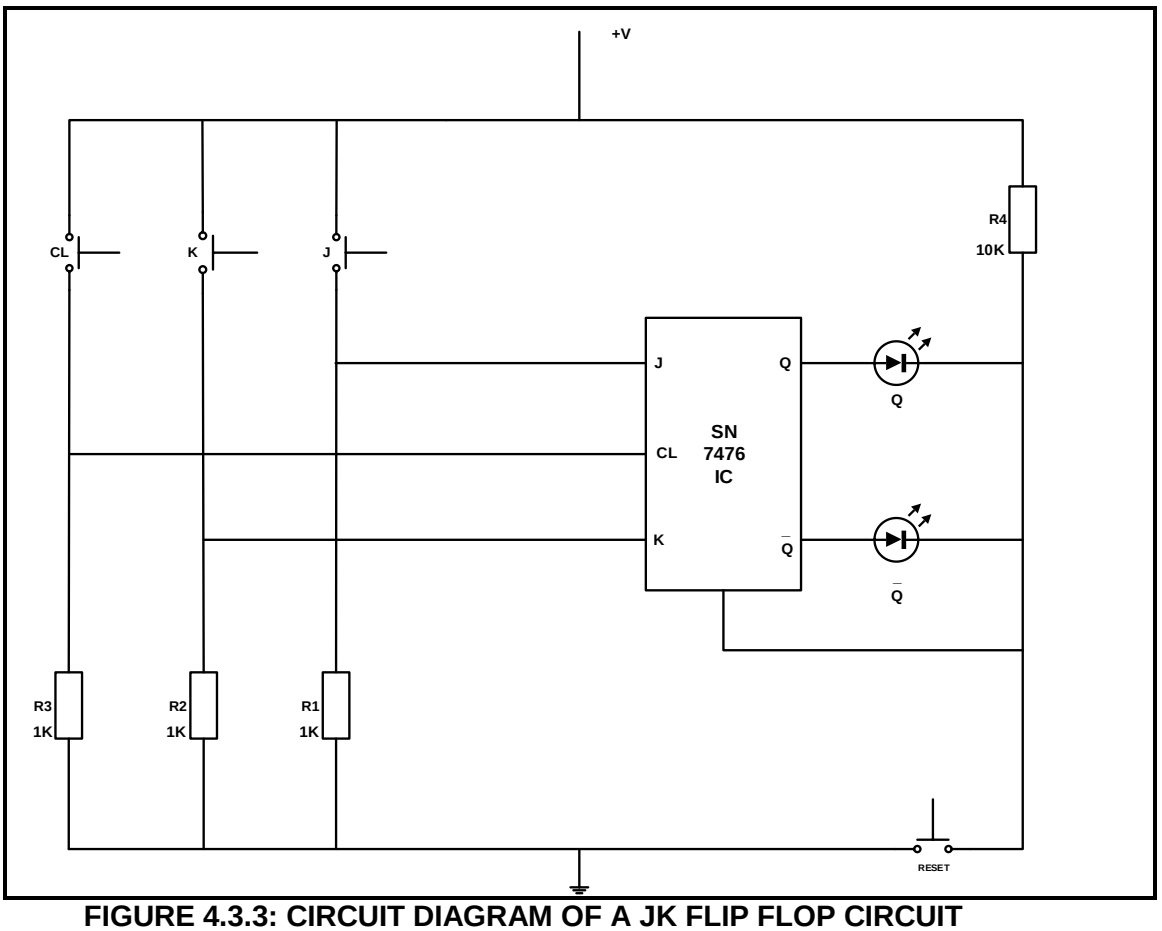


FIGURE 4.3.3: CIRCUIT DIAGRAM OF A JK FLIP FLOP CIRCUIT

4.4.4 **Procedure:**

- Apply logic 0 to J and K input and 1 to the CL, and observe the $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ output
- Apply logic 0 to J and logic 1 to K input and 1 to the CL, and observe the $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ output.
- Apply logic 1 to J and logic 0 to K input and 1 to the CL, and observe the $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ output
- Apply logic 1 to J and logic 1 to K input and 1 to the CL, observe the $\boldsymbol{Q}$ and $\overline{\boldsymbol{Q}}$ output

RUBRIC FOR SIMULATION 4A:

LEVEL DESCRIPTOR				MARK OBTAINED
1	**2**	**3**	**5**	
The learner could not identify the correct components	The learner identified the correct components but could not identify the polarity of the LEDs and the pin out of the IC	The learner identified the correct components and identified the polarity of the LEDs and the pin out of the IC after assistance by the teacher	The learner identified the correct components and identified the polarity of the LEDs and the pin out of the IC without the assistance of the teacher	
The learner could not build the circuit	The learner managed to build the circuit after being assisted by the teacher more than once	The learner managed to build the circuit after being assisted by the teacher once	The learner managed to build the circuit without the assistance of the teacher	

(10)

4.4.5 **Observations:**

(a) Press the J and K switches. Write down your observation. (1)

(b) Press the clock and J switches simultaneously. Write down your observation. (1)

4.4.6 Complete the truth table based on the operation of the circuit you have constructed.

INPUTS			OUTPUTS	
J	K	CL	Q	$\overline{Q}$
0	**0**	**0**		
0	**1**	**0**		
1	**0**	**0**		
1	**1**	**0**		
0	**0**	**1**		
0	**1**	**1**		
1	**0**	**1**		
1	**1**	**1**		

(8)

4.4.7 **Housekeeping**

When you have obtained all the measurements and the teacher has validated all your answer you must tidy up your workplace as part of the safety in the workshop. You will be assessed on housekeeping with the rubric below.

RUBRIC

LEVEL DESCRIPTOR				MARK OBTAINED
0	**2**	**3**	**5**	
The learner did not do any housekeeping.	The learner did housekeeping after the teacher reminded the candidate.	The learner did housekeeping, but only tidied up his/her own workplace and did not help with the cleaning of the rest of the workshop.	The learner did housekeeping on his/her own and helped to tidy up the entire workshop.	

(5)

Simulation 4A: [25]

Simulation 4B: PICAXE

4.4.8 **Purpose:**

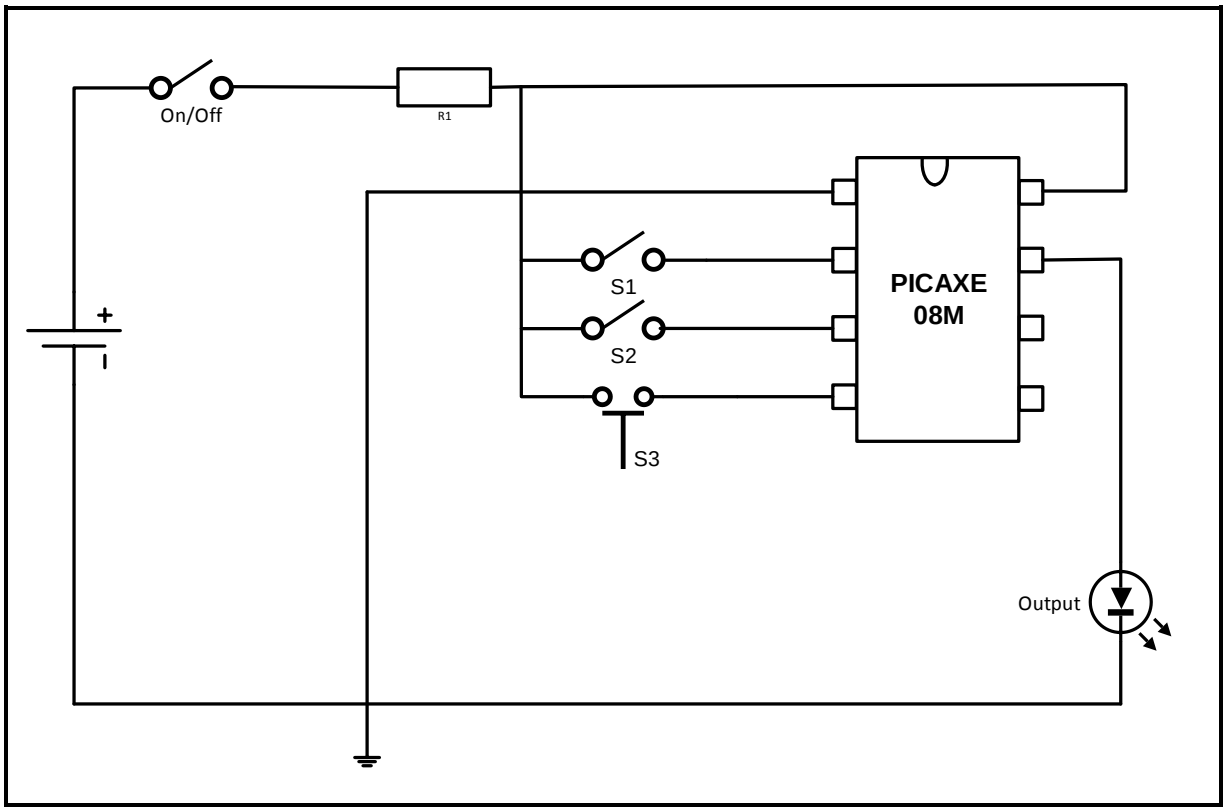
- To test knowledge of flow diagrams and PICAXE.

Study the PICAXE circuit below and design a flow diagram for the circuit.

SCENARIO:

When the on/off switch is activated the program must execute as follows:

(a) S3 must be pushed to activate the OUTPUT LED (the LED will come on for either 5 or 2 seconds). S3 is a push-button.
(b) S2 must be used to select one of TWO timers (one set to 5 seconds and the other to 2 seconds). S2 is a toggle switch.
(c) S1 must allow the user to repeat the program or to stop it. S1 is a toggle switch.



FACET SHEET FOR SIMULATION 4B: PICAXE FLOWCHART

	FACET 1	FACET 2	FACET 3	FACET 4	FACET 5	MAXIMUM POSSIBLE MARKS	LEARNER MARK
Start/Stop element	Start element placed correctly (1)	Stop element placed correctly (1)				**2**	
Decision element	One decision element placed correctly (1)	Two decision elements placed correctly (2)	Three decision elements placed correctly (3)	Four decision elements placed correctly (4)		**4**	
Process element	One process element placed correctly (1)					**1**	
Data elements	One data element placed correctly (1)	Two data elements placed correctly (2)	Three data elements placed correctly (3)	Four data elements placed correctly (4)	Five data elements placed correctly (5)	**5**	
Flow lines	25% of flow lines placed correctly (2)	50% of flow lines placed correctly (4)	75% of flow lines placed correctly (6)	All flow lines placed correctly (9)		**9**	
Labelling of elements	3 labels placed correctly (1)	6 labels placed correctly (2)	9 labels placed correctly (3)	All labels placed correctly (4)		**4**	
				FACET 4B		**25**	

Simulation 4A: (25)
Simulation 4B: (25)
TOTAL: SIMULATION 4: **[50]**

5. SECTION B: DESIGN AND MAKE

Design and Make Project

Time: January to August 2022

Learner Name: _____

School: _____

Class: _____

Title/Type of Project: _____

INSTRUCTIONS

- This section is COMPULSORY for all learners.
- The teacher will choose a circuit for the project.
- Any project constructed must include at least (but is not limited to):
  - Seven components
  - A variety of components (both active and passive)
  - PCB making in some form
  - Soldering
  - An enclosure with a switch and protection
- The checklist below must be used to ensure that all the required tasks for the PAT have been completed.

PAT CHECKLIST

The learner MUST fill in this checklist BEFORE marking of the section takes place.

NO.	DESCRIPTION	TICK (☑)	
		NO	YES
Design and Make: Part 1			
1.	Circuit diagram drawn	☐	☐
2.	Circuit description filled in	☐	☐
3.	Component list completed	☐	☐
4.	Tools list for circuitry populated	☐	☐
5.	Measuring instrument list filled in	☐	☐
Design and Make: Part 2			
1.	Enclosure design completed and included in the file	☐	☐
2.	Unique name written down and on the enclosure	☐	☐
3.	Logo designed and on the enclosure	☐	☐
Miscellaneous			
1.	Enclosure included in the project	☐	☐
2.	Enclosure prepared and drilled according to the design	☐	☐
3.	Enclosure finished off and completed with name and logo	☐	☐
4.	PCB securely mounted in the enclosure using acceptable techniques	☐	☐
5.	Circuit inside the enclosure accessible	☐	☐
6.	Internal wiring neat and ready for inspection	☐	☐
7.	File and project completed and ready for moderation at the workshop/room	☐	☐

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5.1 Design and Make: Part 1

5.1.1 Circuit diagram

Draw a circuit diagram of the project chosen and paste it on the next page.

5.1.2 Project: Description of operation

Use the space below to describe how the project operates. Do research and use your own words.

5.1.3 **Component list**

List the components you will need for the circuit diagram.

LABEL	DESCRIPTION AND VALUE	QUANTITY

5.1.4 **Tools/Instrument List**

List the tools needed to complete the project.

DESCRIPTION	PURPOSE

5.2 Assessment of the design and make phase: Part 1

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = ✗
Circuit Diagram			
1.	The circuit diagram was drawn using EGD equipment.	5	
2.	The circuit diagram was drawn using CAD/any electronic design software.	1	
3.	The circuit diagram was drawn using correct symbols.	3	
4.	The circuit diagram has all labels – R1, C1, Tr1, etc.	3	
5.	The circuit diagram has all component values –100 Ω, 220 µF, etc.	4	
6.	The circuit diagram has a name/title.	2	
7.	The circuit diagram has a frame and title block. (EGD approach).	2	
	Circuit Diagram Subtotal:	**20**	
Component List			
8.	Labels correlate with circuit diagram.	2	
9.	Description and values correlate with circuit diagram.	2	
10.	Quantities are correct.	1	
	Component List Subtotal:	**5**	
Description of Operation			
11.	Basic function of the circuit is described correctly.	10	
12.	All subcircuits in the circuit diagram and component list are included in the description.	5	
13.	Purposes of subcircuits in the circuit diagram are described correctly.	5	
14.	Learner used own interpretation and did not copy from another source verbatim.	4	
15.	Sources are acknowledged.	1	
	Description of Operation Subtotal:	**25**	
Tools/Instrument List			
16.	The tools/instrument list has been completed.	4	
17.	The tools/instruments listed all have a purpose for being used.	1	
	Tools/Instrument List Subtotal:	**5**	

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NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = ✗
Circuit Board Manufacturing			
18.	Transfer of the PCB design onto the blank board is correct. Not over exposed or under exposed.	5	
19.	Circuit board is etched neatly according to the PCB design.	10	
20.	The learner's name is etched onto the circuit design.	4	
21.	All burrs are removed.	2	
22.	Axial and radial components are placed neatly and flush with the board.	5	
23.	Component orientation are aligned between similar components (e.g. the gold band of all resistors are placed on the same side).	2	
24.	Soldered components – leads are cut off, flush and neat on the solder side.	5	
25.	More than 60% of the solder joints are shiny (not dry joints).	5	
26.	Wire insulation is stripped to the correct length (no extra copper showing).	3	
27.	Wiring is long enough to allow for dismantling and inspection.	2	
28.	Wiring is wrapped neatly.	2	
29.	A power switch is included and fitted to the enclosure.	2	
30.	Wiring entering/exiting the enclosure is provided with a grommet/applicable fittings/sockets where applicable.	2	
31.	A fuse/Protection is included and fitted correctly where applicable.	2	
32.	Batteries/Transformer is mounted using a battery housing/ mounting bracket and battery clip (NO double-sided tape).	2	
33.	The project has a pilot light/LED installed in the enclosure showing when the circuit is operational. LED is mounted with a grommet or applicable fitting. (Switch is on – must go out when fuse is blown.)	2	
34.	The project is fully operational and commissioned/installed in the enclosure.	10	
	Circuit Board Manufacturing Subtotal:	**65**	
	Circuit Diagram Subtotal:	**20**	
	Component List Subtotal:	**5**	
	Description of Operation Subtotal:	**25**	
	Tools/Instrument List Subtotal:	**5**	
	Circuit Board Manufacturing Subtotal:	**65**	

TOTAL (PART 1 = 120 marks)	

NOTE: In projects where facets are not applicable, the projects should be marked and the totals adjusted accordingly.

5.3 Design and Make: Part 2

5.3.1 Enclosure design

- Design an enclosure for your project.
- NO FREEHAND DRAWINGS.
- Draw using EGD equipment **OR** use a CAD program.
- Draw in first-angle orthographic projection.
- Add your drawings after this page.
- Use colour to enhance your drawing.

5.3.2 Manufacture the enclosure neatly according to your design.
You may use pre-cut panels from metal, wood and/or Perspex/Plexiglass. You must, however, construct/assemble these parts.
Injection moulded enclosures are also acceptable. It is important that your enclosure and the placement of the parts align with your design.

5.3.3 Choose a name for your device.
Write down the name of the device below.

_____

5.3.4 Design a unique logo for your device, as well as a specification plate and attach it after this page. **[30]**

5.4 Assessment of the Design-and-Make-Phase: Part 2

NO.	FACET DESCRIPTION	Mark	Achieved = 1 Not achieved = ✖
Enclosure Design			
1.	Enclosure design is included in first-angle orthographic projection.	2	
2.	Drawn design includes a title box and page border.	1	
3.	Isometric drawing included additionally.	2	
4.	Dimensions are included.	2	
5.	The name of the device is written in the PAT document.	1	
6.	The logo design and specification plate design is in the PAT document.	2	
	Enclosure Design Subtotal:	**10**	
Enclosure Manufacturing			
7.	Enclosure matches the design. – Dimensions and placement correlate.	1	
8.	Name of the device is attached on the enclosure.	1	
9.	The logo design is attached on the enclosure.	2	
10.	The logo design on the enclosure is durable and not merely a paper pasted on the enclosure (painted/used decoupage/screen printed/sublimation printed).	2	
11.	The enclosure is manufactured from scratch/pre-cut parts. Does NOT include: cardboard, paper, margarine container Does include: sheet metal, Perspex, Plexiglas, wood, glass and other raw materials, injection-moulded plastic boxes	5	
12.	Holes/Cut-outs in the enclosure are made with the appropriate tools.	3	
13.	Specification plate with the learner's name, operating voltage, fuse rating and additional information on the project.	2	
14.	Enclosure is neatly prepared, painted and aesthetically pleasing.	2	
15.	The circuit board is mounted using appropriate methods inside the enclosure. (NO double-sided tape, Prestik, glue, chewing gum, masking tape, etc.)	2	
	Enclosure Manufacturing Subtotal:	**20**	

TOTAL (PART 2 = 30 marks)	

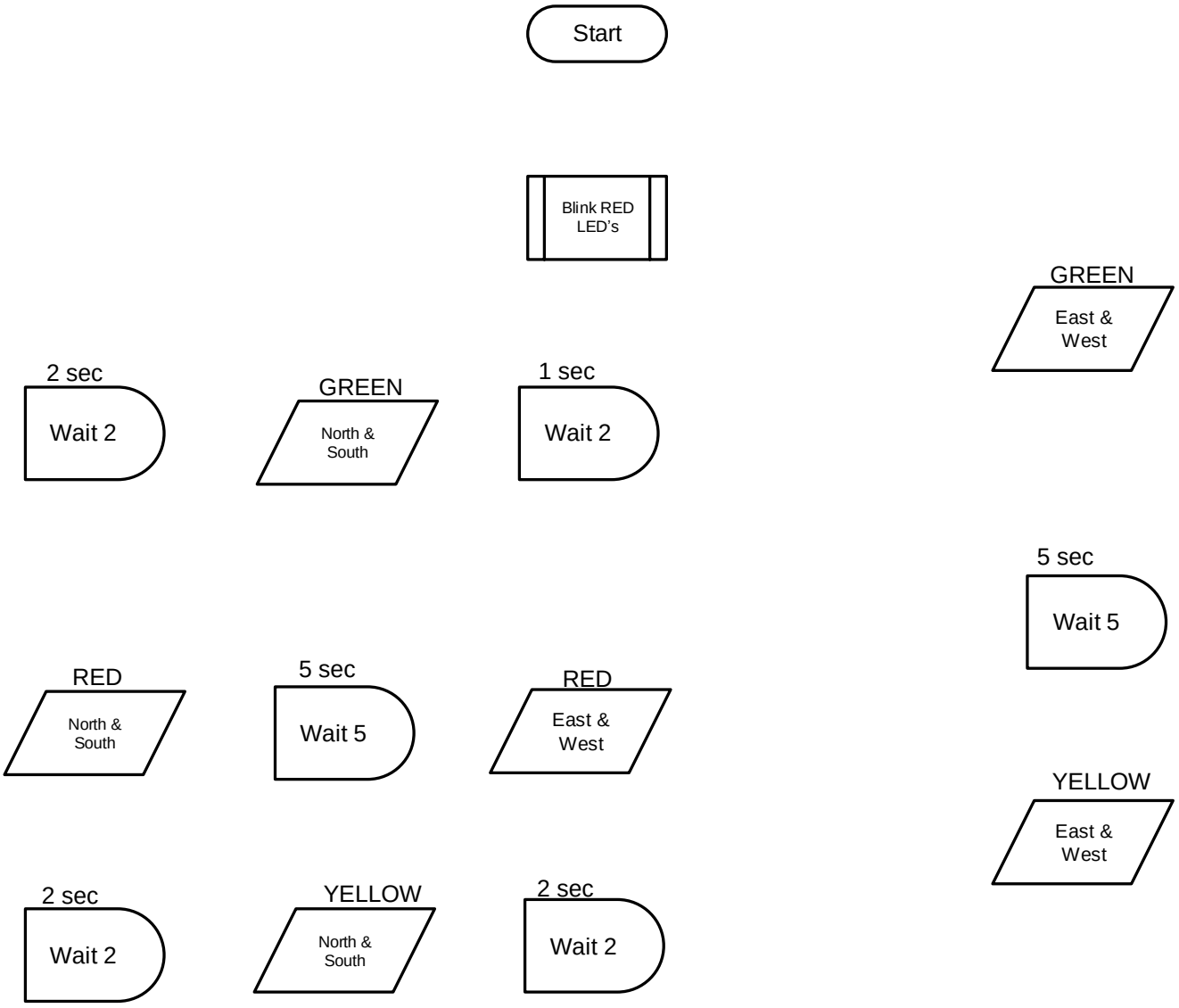
6. PROJECTS

6.1 Practical Project: Traffic Light

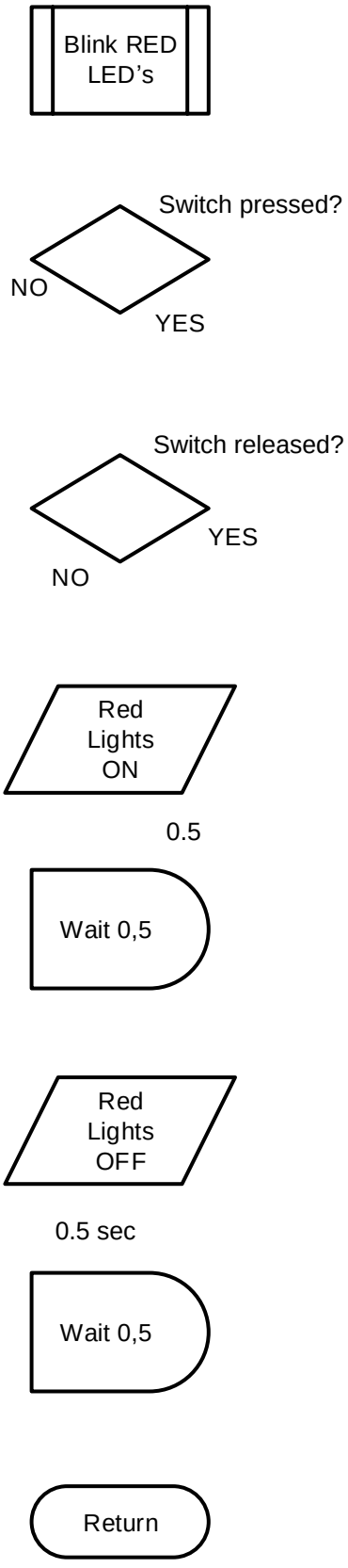
This project operates red, yellow/amber and green LEDs in the correct sequence for traffic lights at a four-way crossing. The traffic lights start by blinking all red lights and allowing all red lights to stay on. The east and west green lights will be switched first. The delays between green to yellow/amber and between yellow to red are 5 and 2 seconds respectively. The PICAXE 18m2 is used to control the traffic lights.

Refer to the incomplete flowchart below and complete the flow of the program.

FLOWCHART: TRAFFIC LIGHTS



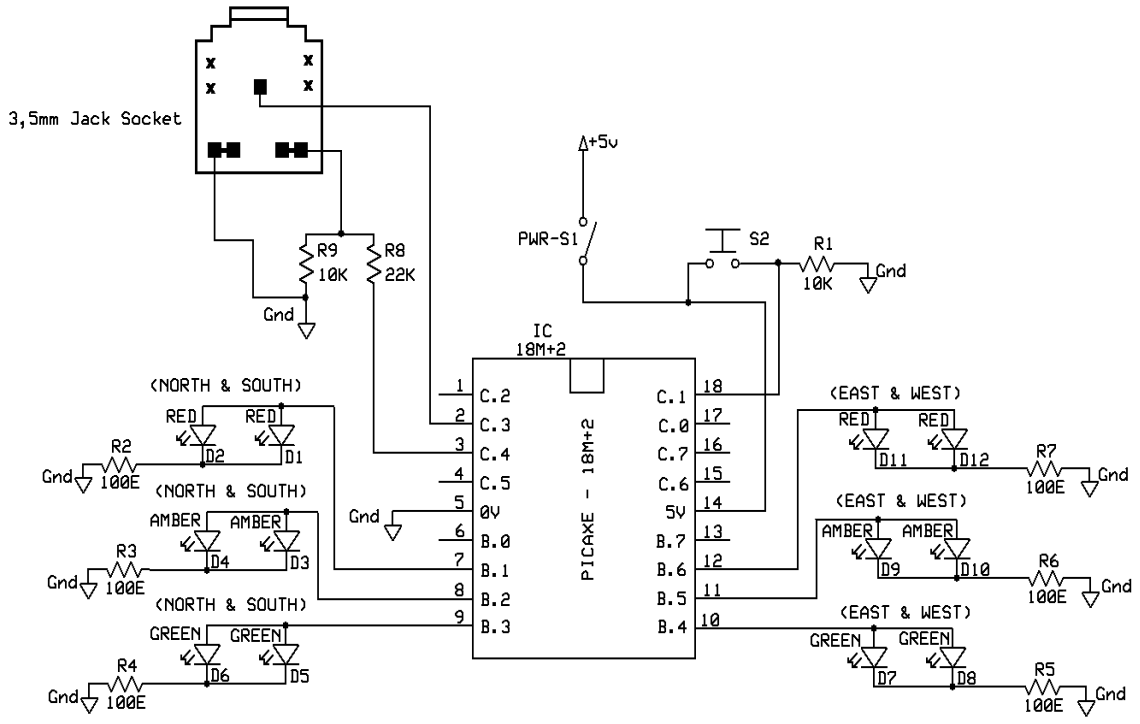
(continues on next page)


Blink RED LED's
Switch pressed?
NO
YES
Switch released?
YES
NO
Red Lights ON
0.5
Wait 0,5
Red Lights OFF
0.5 sec
Wait 0,5
Return

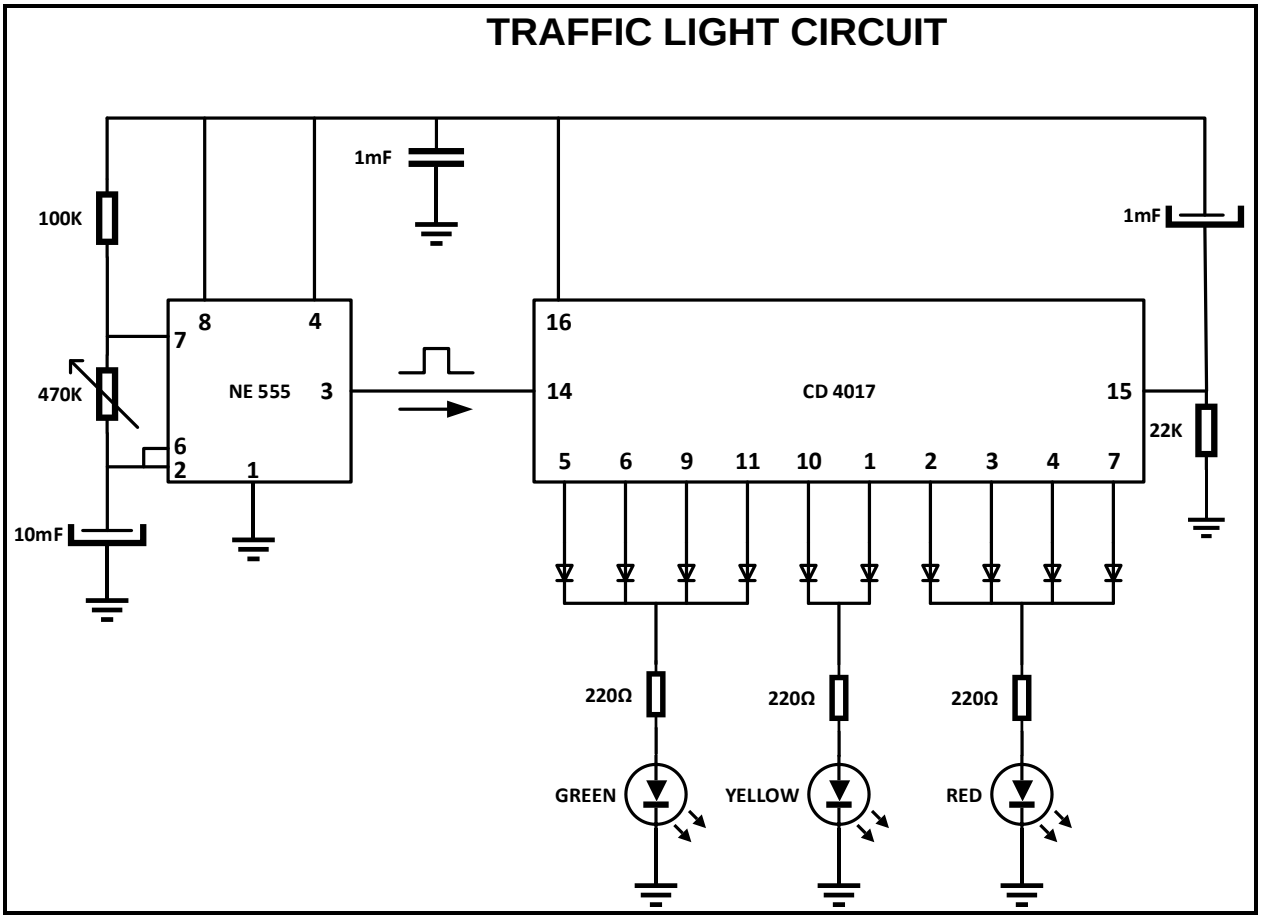
COMPONENT LIST

TOOLS/INSTRUMENTS	MATERIALS
• Laptop/desktop computer • Picaxe Editor6 software • Picaxe download cable (AXE027) • Oscilloscope (analogue/digital) • Analogue/Digital trainer with dual power supply • Electronics multimeter • Soldering iron • Helping hands • PCB etching tank or similar • Solder sucker • Wire stripper • Side cutters	• 10 kΩ resistor x 2 • 22 kΩ resistor x 1 • 100 Ω resistor x 6 • LED green x 4 • LED yellow x 4 • LED red x 4 • SPST switch x 1 • Press-to-make switch x 1 • IC 18M+2 Picaxe • 3,5 mm Stereo Jack Socket • PCB 150 x 100 mm • Solder • PCB etching chemicals

CIRCUIT DIAGRAM



ALTERNATIVE CIRCUIT DIAGRAM:



TRAFFIC LIGHT CIRCUIT

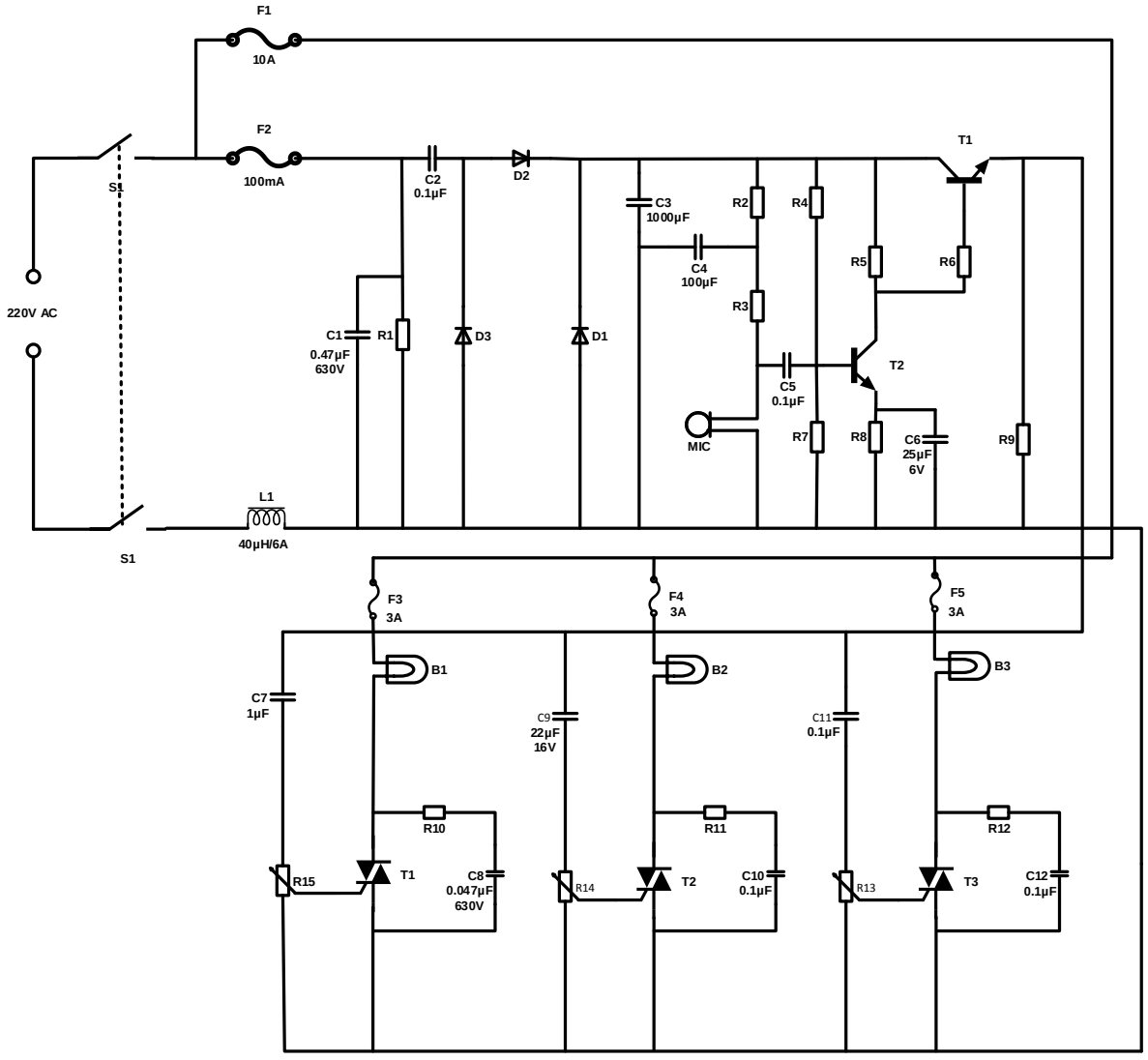
COMPONENT LIST		
RESISTORS	**CAPACITORS**	**DIODES**
R1 100 k Ω	C1 1 µF	LED GREEN
R2 220 Ω	C2 1 µF	LED YELLOW
R3 220 Ω	C3 10 µF	LED RED
R4 220 Ω		D1 1N4007 X 6
R5 22 kΩ		IC CD 4017
R6 470 kΩ (Adjustable resistor)		IC NE555

6.2 Practical project: Sound-to-light controller

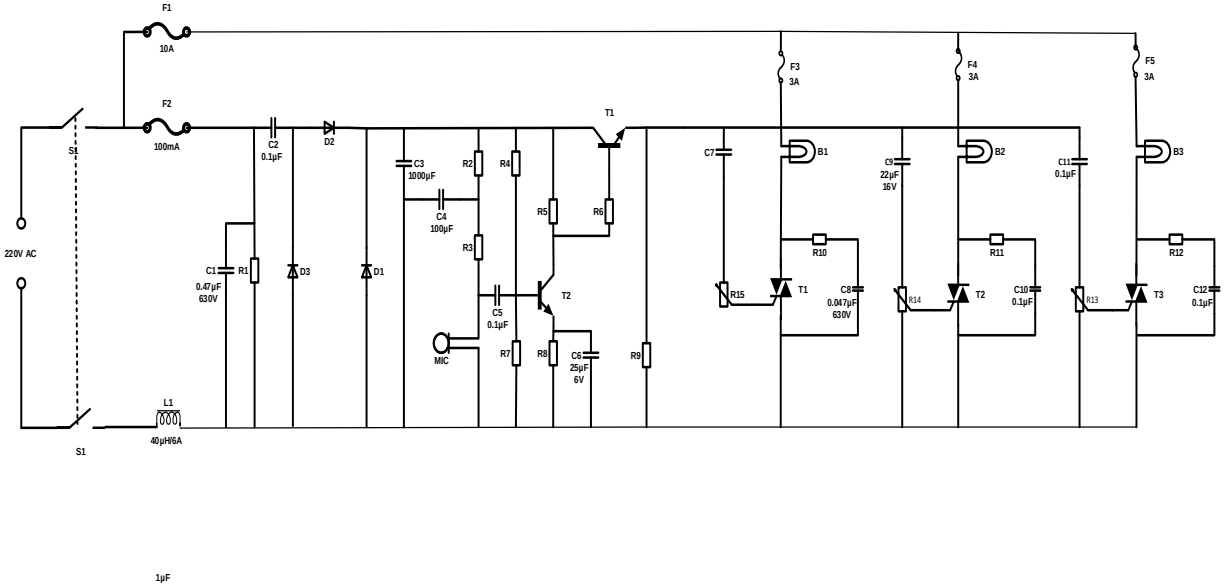
This sound-controlled lights circuit design is used to control the brightness of the lights attached to it in sync with the sound that is being captured by its microphone. This electronic circuit design is very common in discos, bars, at parties.

Usually sound-controlled lights are just connected in parallel with the loudspeakers. This configuration has two disadvantages: a very powerful amplifier can destroy the lights or, even worse, a defective light can destroy the amp. This problem is avoided by the circuit by not being connected directly to the amp. Instead, it picks up the sound with its microphone.

The power supply part is on the left of the electret microphone amplifier and the light controller part is on the right. The capacitors C2 and C3 are the capacitive voltage dividers and reduce the power supply level. Diodes D1 and D2 rectify the positive swing of the AC voltage. The network, composed of L1 and C1, protects the power line from voltages surges. In this circuit design, an electret microphone is used. Take note that there are two types of electret mics. The first type has three pins for power, ground, and output. The second type has only two pins. The second type is used for this circuit.



SOUND-TO-LIGHT CONTROLLER



SOUND-TO-LIGHT CONTROLLER CIRCUIT

COMPONENT LIST	
R1 =560 kΩ/1 W	C8, C12 = 0,047 µF/630 V
R2, R3 = 15 kΩ ¼ W	C9 = 22 µF 16 V
R4 = 33 kΩ /¼ W	C11 = 47 µF 16 V
R5, R6, R9 = 1 kΩ ¼ W	D1, D2 = 1N4004
R7 =18 kΩ ¼ W	D3 = 1N4742 12v/1 W
R8 = 560 Ω ¼ W	F1 10 A fuse 220 V
R10, R11, R12 =100 kΩ	F2 100 mA fuse 220 V
P1, P2, P3 = 5 kΩ Pot	F3, F4, F5 220 V 3 A fuse
C1 = 0,47 uF 630 V	L1 = 40 µH 6 A
C2, C5 0,1 µF/220 V	B1, B2, B3 = 60 W incandescent lamp
C3 1 000 µF/16 V	Mic = low-impedance microphone
C4 100 µF/16 V	
C6 25 µF/6 V	
C7 1 µF 16 V	

WARNING: Some parts in the circuit board are subject to lethal potential because the device is connected to 230 V AC. When plugging in the project, place it in a plastic or wooden box to prevent the circuit from shocking you. Avoid connecting this circuit to other appliances (e.g. to the output of an amplifier by means of a cable) because of the absence of a mains transformer. Use only the microphone in the main case to pick up the sound.

7. CONCLUSION

On completion of the practical assessment task learners should be able to demonstrate their understanding of the industry, enhance their knowledge, skills, values and reasoning abilities as well as establish connections to life outside the classroom and address real-world challenges. The PAT furthermore develops learners' life skills and provides opportunities for learners to engage in their own learning.

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